8224
CLOCK GENERATOR AND DRIVER FOR 8080A CPU

- **Single Chip Clock Generator/Driver for 8080A CPU**
- **Power-Up Reset for CPU**
- **Ready Synchronizing Flip-Flop**
- **Advanced Status Strobe**
- **Oscillator Output for External System Timing**
- **Crystal Controlled for Stable System Operation**
- **Reduces System Package Count**
- **Available in EXPRESS — Standard Temperature Range**
- **Available in 16-Lead Cerdip Package**
  (See Packaging Spec, Order #231369)

The Intel 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer to meet a variety of system speed requirements.

Also included are circuits to provide power-up reset, advance status strobe, and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

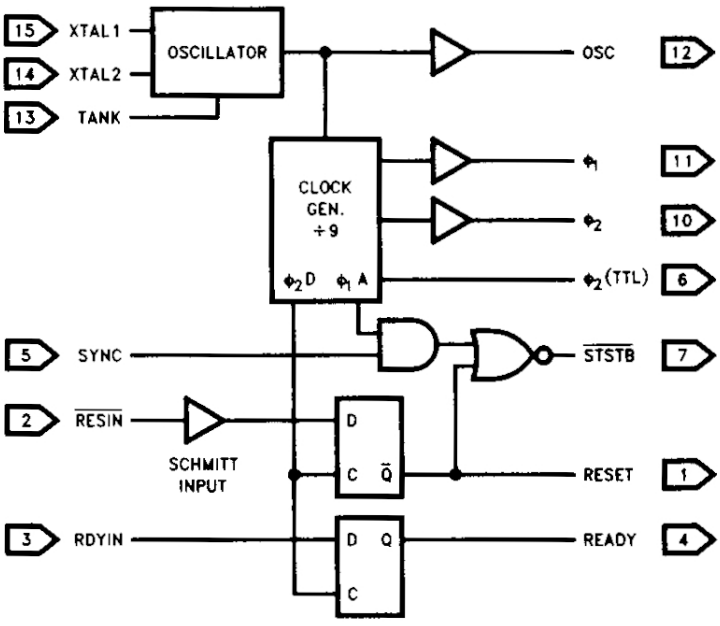

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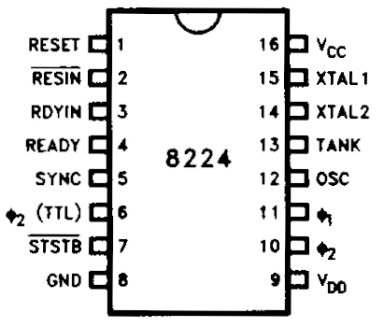
Figure 1. Block Diagram



231464-2

RESIN	Reset Input
RESET	Reset Output
RDYIN	Ready Input
READY	Ready Output
SYNC	Sync Input
STSTB	Status STB (Active Low)
ϕ_1	8080 Clocks
ϕ_2	8080 Clocks

XTAL 1	Connections for Crystal
XTAL 2	Connections for Crystal
TANK	Used with Overtone XTAL
OSC	Oscillator Output
ϕ_2 (TTL)	ϕ_2 CLK (TTL Level)
V_{CC}	+5V
V_{DD}	+12V
GND	0V

Figure 2. Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Supply Voltage, V_{CC} ..... −0.5V to +7V
Supply Voltage, V_{DD} ..... −0.5V to +13.5V
Input Voltage ..... −1.5V to +7V
Output Current ..... 100 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%, V_{DD} = +12V ±5%

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
I_F	Input Current Loading			−0.25	mA	V_F = 0.45V
I_R	Input Leakage Current			10	μA	V_R = 5.25V
V_C	Input Forward Clamp Voltage			1.0	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.6			V	Reset Input
		2.0			V	All Other Inputs
$V_{IH}-V_{IL}$	RESIN Input Hysteresis	0.25			V	V_{CC} = 5.0V
V_{OL}	Output "Low" Voltage			0.45	V	(ϕ_1, ϕ_2), Ready, Reset, $\overline{STSTB}$ I_{OL} = 2.5 mA
				0.45	V	All Other Outputs I_{OL} = 15 mA
V_{OH}	Output "High" Voltage ϕ_1, ϕ_2	9.4			V	I_{OH} = −100 μA
	READY, RESET	3.6			V	I_{OH} = −100 μA
	All Other Outputs	2.4			V	I_{OH} = −1 mA
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

NOTE:
1. For crystal frequencies of 18 MHz connect 510Ω resistors between the X1 input and ground as well as the X2 input and ground to prevent oscillation at harmonic frequencies.

Crystal Requirements

Tolerance: 0.005% at 0°C–70°C
Resonance: Series (Fundamental)*
Load Capacitance: 20 pF–35 pF
Equivalent Resistance: 75Ω–20Ω
Power Dissipation (Min): 4 mW

***NOTE:**
With tank circuit use 3rd overtone mode.

A.C. CHARACTERISTICS

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2tcy}{9} - 20$ ns			ns	C_L = 20 pF to 50 pF
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5tcy}{9} - 35$ ns				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2tcy}{9} - 14$ ns				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2tcy}{9}$		$\frac{2tcy}{9} + 20$ ns		
t_R	ϕ_1 and ϕ_2 Rise Time			20		
t_F	ϕ_1 and ϕ_2 Fall Time			20		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	−5		+15	ns	ϕ_2 TTL, CL = 30 R_1 = 300Ω R_2 = 600Ω
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\frac{6tcy}{9} - 30$ ns		$\frac{6tcy}{9}$	ns	$\overline{STSTB}$, C_L = 15 pF R_1 = 2K R_2 = 4K
t_{PW}	$\overline{STSTB}$ Pulse Width	$\frac{tcy}{9} - 15$ ns			ns	
t_{DRS}	RDYIN Setup Time to Status Strobe	$50\text{ ns} - \frac{4tcy}{9}$				
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	$\frac{4tcy}{9}$				
t_{DR}	RDYIN or RESIN to ϕ_2 Delay	$\frac{4tcy}{9} - 25$ ns			ns	Ready & Reset C_L = 10 pF R_1 = 2K R_2 = 4K
t_{CLK}	CLK Period		$\frac{tcy}{9}$		ns	
f_{max}	Maximum Oscillating Frequency			27	MHz	
C_{in}	Input Capacitance			8	pF	V_{CC} = +5.0V V_{DD} = +12V V_{BIAS} = 2.5V f = 1 MHz

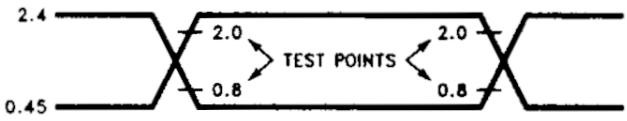
NOTE:
These formulas are based on the internal workings of the part and intended for customer convenience. Actual testing of the part is done at t_{cy} = 488.28 ns.

A.C. CHARACTERISTICS (Continued)

For t_{CY} = 488.28 ns; T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%

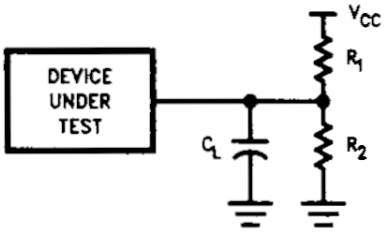
Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	t_{CY} = 488.28 ns
$t_{\phi 2}$	ϕ_2 Pulse Width	236			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	95			ns	ϕ_1 & ϕ_2 Loaded to C_L = 20 pF to 50 pF
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		129	ns	
t_r	Output Rise Time			20	ns	
t_f	Output Fall Time			20	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	−5		+15	ns	
t_{PW}	Status Strobe Pulse Width	40			ns	Ready & Reset Loaded to 2 mA/10 pF All measurements referenced to 1.5V unless specified otherwise.
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	−167			ns	
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	
f_{MAX}	Oscillator Frequency			18.432	MHz	

A.C. TESTING, INPUT, OUTPUT WAVEFORM



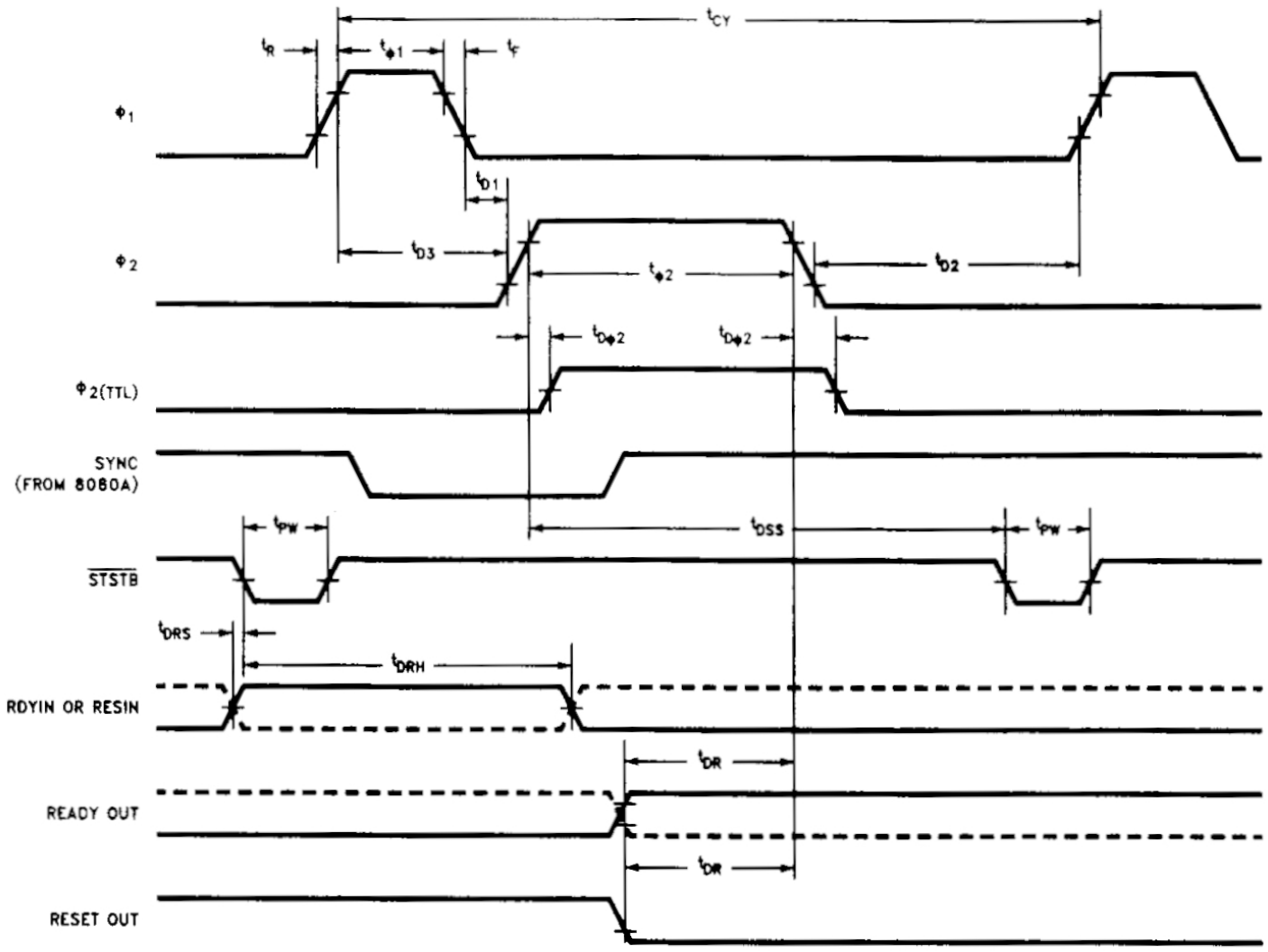
A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0" (unless otherwise noted).

A.C. TESTING LOAD CIRCUIT



C_L Includes Jig Capacitance

WAVEFORMS



VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V. All other signals measured at 1.5V.

CLOCK HIGH AND LOW TIME (USING X1, X2)