PROGRAMMABLE INTERRUPT CONTROLLER

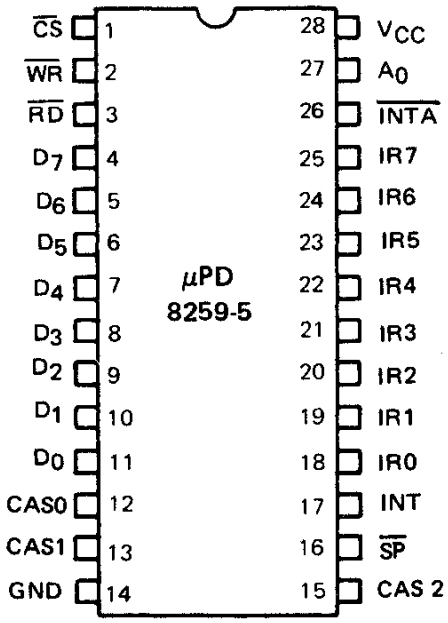
DESCRIPTION

The NEC μPD8259-5 is a programmable interrupt controller directly compatible with the 8080A/8085A/μPD780(Z80™). It can service eight levels of interrupts and contains on-chip logic to expand interrupt capabilities up to sixty-four levels with the addition of other μPD8259-5's. The user is offered a selection of priority algorithms to tailor the priority processing to meet his systems requirements. These algorithms can be dynamically modified during operation, expanding the versatility of the microprocessor system.

FEATURES

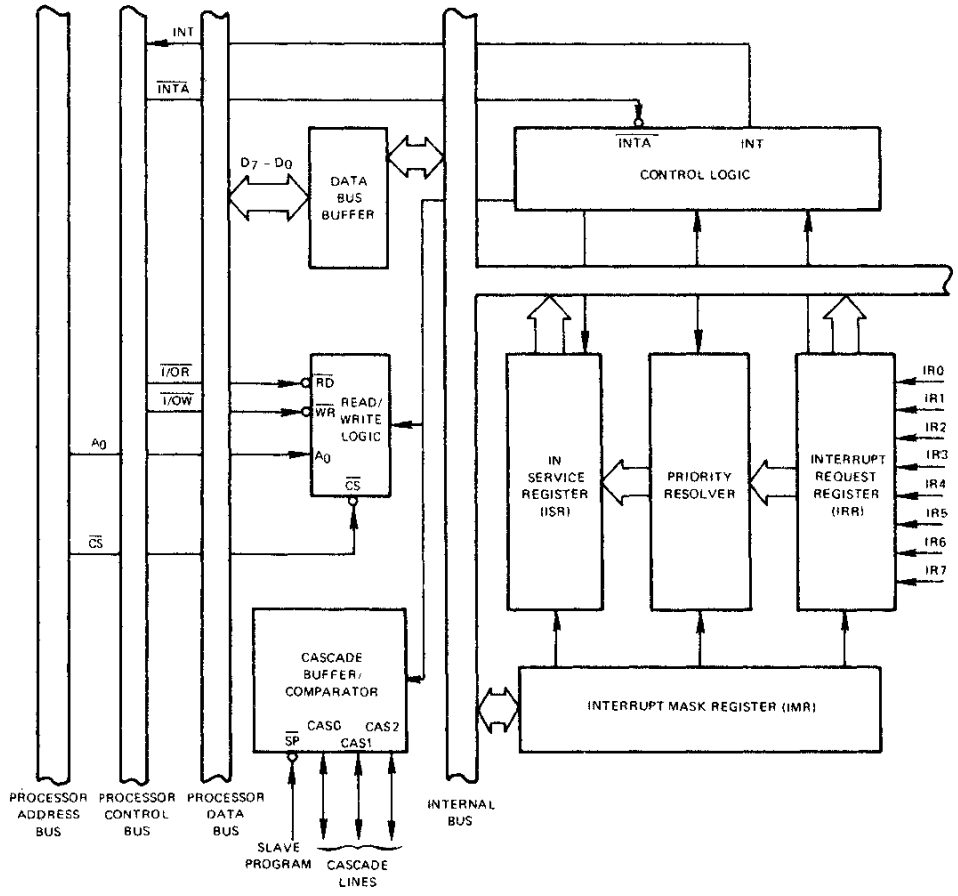
- NEC now Supplies μPD8259-5 to μPD8259 Requirements
- Eight Level Priority Controller
- Programmable Base Vector Address
- Expandable to 64 Levels
- Programmable Interrupt Modes (Algorithms)
- Individual Request Mask Capability
- Single +5V Supply ±10% (No Clocks)
- Full Compatibility with 8080A
- μPD8259-5 Compatible with 8085A Speeds
- Available in 28 Pin Plastic and Ceramic Packages

PIN CONFIGURATION



PIN NAMES

$D_7 - D_0$	Data Bus (Bi-Directional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Command Select Address
CAS2 – CAS0	Cascade Lines
$\overline{SP}$	Slave Program Input
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0 – IR7	Interrupt Request Inputs
$\overline{CS}$	Chip Select



Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Voltage on Any Pin . . . . . −0.5 to +7 Volts (1)
Power Dissipation 1W

Note: (1) With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5V	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Interrupt Output-High Voltage	V_{OH-INT}	2.4			V	I_{OH} = −400 μA
		3.5			V	I_{OH} = −50 μA
Input Leakage Current for IR_{0-7}	I_{IL} (IR_{0-7})			−300	μA	V_{IN} = 0V
				10	μA	V_{IN} = V_{CC}
Input Leakage Current for other Inputs	I_{IL}			±10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{LOL}			− 10	μA	V_{OUT} = 0.45 V
Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Supply Current	I_{CC}			85	mA	

$T_a = 25°C$; $V_{CC} = GND = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured Pins Returned to V_{SS}

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$; GND = 0V

PARAMETER	SYMBOL	LIMITS ② 8259 MIN	LIMITS ② 8259 MAX	LIMITS 8259-5 MIN	LIMITS 8259-5 MAX	UNIT	TEST CONDITIONS
READ							
$\overline{CS}/A_0$ Stable Before $\overline{RD}$ or $\overline{INTA}$	t_{AR}	50		0		ns	
$\overline{CS}/A_0$ Stable After $\overline{RD}$ or $\overline{INTA}$	t_{RA}	50		0		ns	
$\overline{RD}$ Pulse Width	t_{RR}	420		250		ns	
Data Valid From $\overline{RD}/\overline{INTA}$	t_{RD}		300		150	ns	①
Data Float After $\overline{RD}/\overline{INTA}$	t_{DF}	20	200	20	100	ns	①
WRITE							
A_0 Stable Before $\overline{WR}$	t_{AW}	50		0		ns	
A_0 Stable After $\overline{WR}$	t_{WA}	20		0		ns	
$\overline{CS}$ Stable Before $\overline{WR}$	t_{CW}	50				ns	
$\overline{CS}$ Stable After $\overline{WR}$	t_{WC}	20				ns	
$\overline{WR}$ Pulse Width	t_{WW}	400		250		ns	
Data Valid to $\overline{WR}$ (T.E.)	t_{DW}	300		150		ns	
Data Valid After $\overline{WR}$	t_{WD}	40		0		ns	
OTHER							
Width of Interrupt Request Pulse	t_{IW}	100		100		ns	
INT ↑ After IR ↑	t_{INT}	400		250		ns	
Cascade Line Stable After $\overline{INTA}$ ↑	t_{IC}	400		300		ns	

Note: ① For μPD8259: C_L = 100 pf; for μPD8259-5: C_L = 150 pf

② Data for Comparison only

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupt request register and in-service register store the in-coming interrupt request signals appearing on the IR0-7 lines (refer to functional block diagram). The inputs requesting service are stored in the IRR while the interrupts actually being serviced are stored in the ISR.

A positive transition on an IR input sets the corresponding bit in the Interrupt Request Register, and at the same time the INT output of the μPD8259-5 is set high. The IR input line must remain high until the first INTA input has been received. Multiple, non-masked interrupts occurring simultaneously can be stored in the IRR. The incoming $\overline{\text{INTA}}$ sets the appropriate ISR bit (determined by the programmed interrupt algorithm) and resets the corresponding IRR bit. The ISR bit stays high-active during the interrupt service subroutine until it is reset by the programmed End-of-Interrupt (EOI) command.

PRIORITY RESOLVER

The priority resolver decides the priority of the interrupt levels in the IRR. When the highest priority interrupt is determined it is loaded into the appropriate bit of the In-Service register by the first $\overline{\text{INTA}}$ pulse.

DATA BUS BUFFER

The 3-state, 8-bit, bi-directional data bus buffer interfaces the μPD8259-5 to the processor's system bus. It buffers the Control Word and Status Data transfers between the μPD8259-5 and the processor bus.

READ/WRITE LOGIC

The read/write logic accepts processor data and stores it in its Initialization Command Word (ICW) and Operation Command Word (OCW) registers. It also controls the transfer of the Status Data to the processor's data bus.

CHIP SELECT ($\overline{\text{CS}}$)

The μPD8259-5 is enabled when an active-low signal is received at this input. Reading or writing of the μPD8259-5 is inhibited when it is not selected.

WRITE ($\overline{\text{WR}}$)

This active-low signal instructs the μPD8259-5 to receive Command Data from the processor.

READ ($\overline{\text{RD}}$)

When an active-low signal is received on the $\overline{\text{RD}}$ input, the status of the Interrupt Request Register, In-Service Register, Interrupt Mask Register or binary code of the Interrupt Level is placed on the data bus.

INTERRUPT (INT)

The interrupt output from the μPD8259-5 is directly connected to the processor's INT input. The voltage levels of this output are compatible with the 8080/8085 input voltage and timing requirements.

INTERRUPT MASK REGISTER (IMR)

The interrupt mask register stores the bits for the individual interrupt bits to be masked. The IMR masks the data in the ISR. Lower priority lines are not affected by masking a higher priority line.

INTERRUPT ACKNOWLEDGE ($\overline{INTA}$)

The interrupt acknowledge signal is usually received from the 8228 (system controller for the 8080A). The system controller generates three INTA pulses to signal the 8259-5 to issue a 3-byte CALL instruction onto the data bus.

A_0

A_0 is usually connected to the processor's address bus. Together with $\overline{WR}$ and $\overline{RD}$ signals it directs the loading of data into the command register or the reading of status data. The following table illustrates the basic operations performed. Note that it is divided into three functions: Input, Output and Bus Disable distinguished by the $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ inputs.

μPD8259 BASIC OPERATION						
A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	PROCESSOR INPUT OPERATION (READ)
0			0	1	0	IRR, ISR or IR → Data Bus ①
1			0	1	0	IMR → Data Bus
						PROCESSOR OUTPUT OPERATION (WRITE)
0	0	0	1	0	0	Data Bus → OCW2
0	0	1	1	0	0	Data Bus → OCW3
0	1	X	1	0	0	Data Bus → ICW1
1	X	X	1	0	0	Data Bus → OCW1, ICW2, ICW3 ②
						DISABLE FUNCTION
X	X	X	1	1	0	Data Bus → 3-State
X	X	X	X	X	1	Data Bus → 3-State

Notes: ① The contents of OCW2 written prior to the READ operation governs the selection of the IRR, ISR or Interrupt Level.

② The sequencer logic on the μPD8259-5 aligns these commands in the proper order.

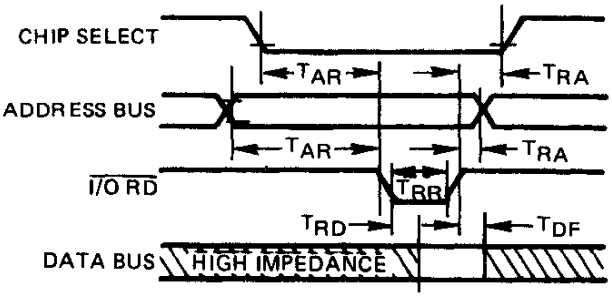
CASCADE BUFFER/COMPARATOR. (For Use in Multiple μPD8259-5 Array.)

The ID's of all μPD8259-5's are buffered and compared in the cascade buffer/comparator. The master μPD8259-5 will send the ID of the interrupting slave device along the CAS0, 1, 2 lines to all slave devices. The cascade buffer/comparator compares its preprogrammed ID to the CAS0, 1, 2 lines. The next two $\overline{INTA}$ pulses strobe the preprogrammed, 2 byte CALL routine address onto the data bus from the slave whose ID matches the code on the CAS0, 1, 2 lines.

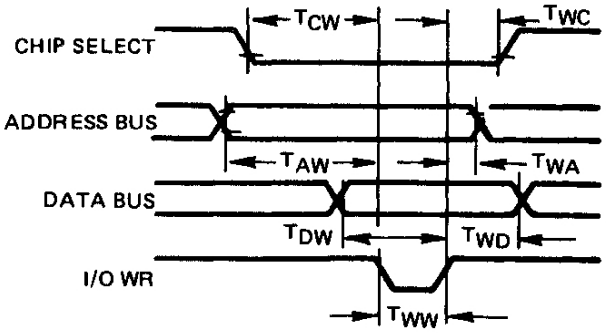
SLAVE PROGRAM ($\overline{SP}$). (For Use in Multiple μPD8259 Array.)

The interrupt capability can be expanded to 64 levels by cascading multiple μPD8259-5's in a master-plus-slaves array. The master controls the slaves through the CAS0, 1, 2 lines. The SP input to the device selects the CAS0-2 lines as either outputs (SP=1) for the master or as inputs (SP=0) for the slaves. For one device only the SP must be set to a logic "1" since it is functioning as a master.

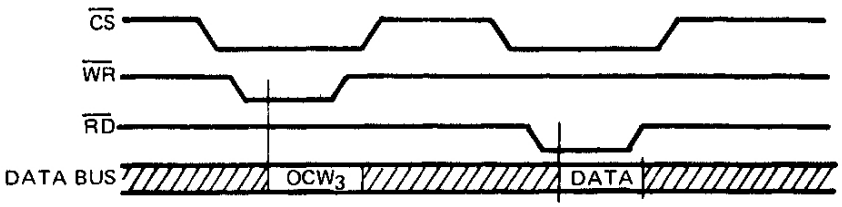
READ



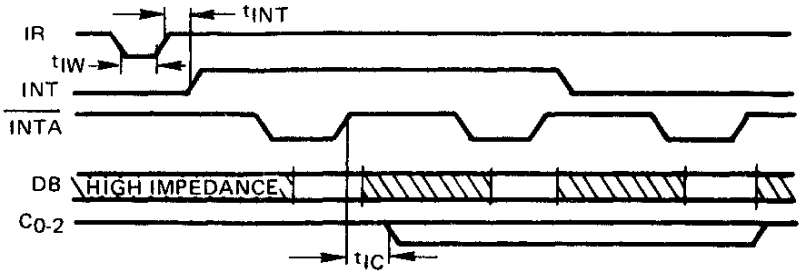
WRITE



READ STATUS/POLL MODE

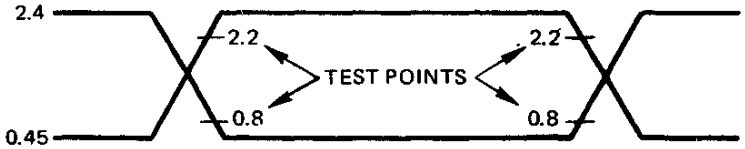


OTHER

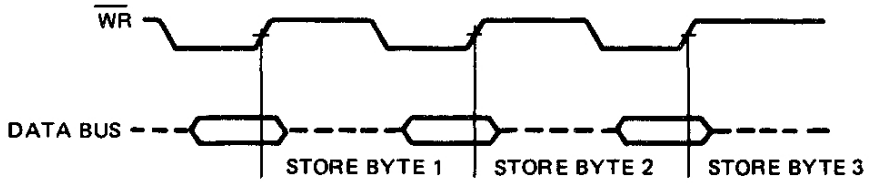


Note: IR must stay "high" at least until the leading edge of 1st $\overline{INTA}$.

INPUT WAVEFORMS FOR AC TESTS



INITIALIZATION SEQUENCE



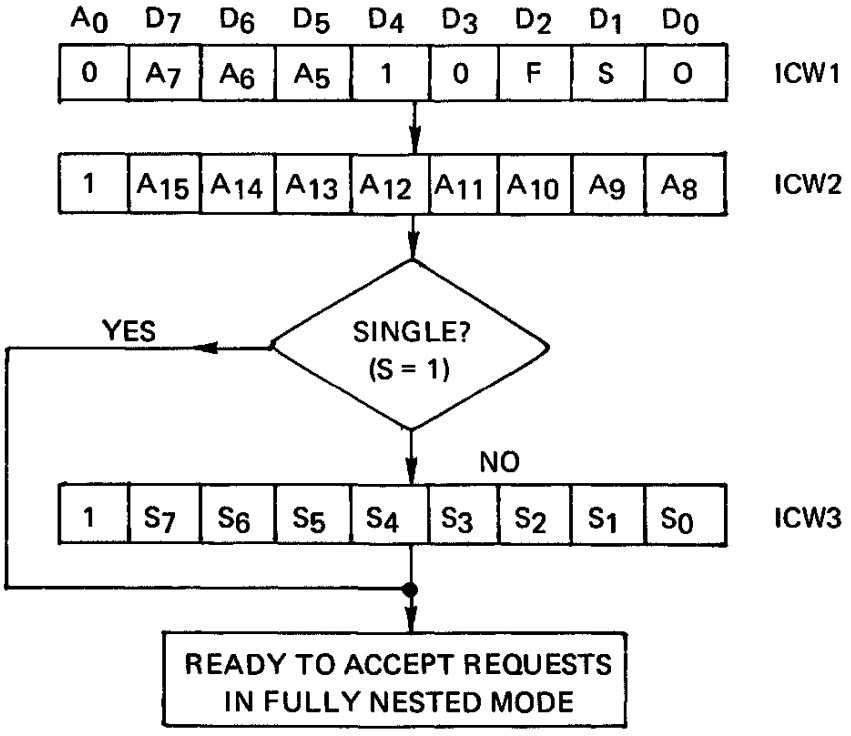
The μPD8259-5 derives its versatility from its programmable interrupt modes and its ability to jump to any memory address through programmable CALL instructions. The following sequence demonstrates how the μPD8259-5 interacts with the processor.

1. An interrupt or interrupts appearing on IR_{0-7} sets the corresponding IR bit(s) high. This in turn sets the corresponding IRR bit(s) high.
2. Once the IRR bit(s) has been set, the μPD8259-5 will resolve the priorities according to the preprogrammed interrupt algorithm. It then issues an INT signal to the processor.
3. The processor group issues an $\overline{\text{INTA}}$ to the μPD8259-5 when it receives the INT.
4. The $\overline{\text{INTA}}$ input to the μPD8259-5 from the processor group sets the highest priority ISR bit and resets the corresponding IRR bit. The INTA also signals the μPD8259-5 to issue an 8-bit CALL instruction op-code (11001101) onto its Data bus lines.
5. The CALL instruction code instructs the processor group to issue two more INTA pulses to the μPD8259-5.
6. The two $\overline{\text{INTA}}$ pulses signal the μPD8259-5 to place its preprogrammed interrupt vector address onto the Data bus. The first $\overline{\text{INTA}}$ releases the low-order 8-bits of the address and the second $\overline{\text{INTA}}$ releases the high-order 8-bits.
7. The μPD8259-5's CALL instruction sequence is complete. A preprogrammed EOI (End-of-Interrupt) command is issued to the μPD8259-5 at the end of an interrupt service routine to reset the ISR bit and allow the μPD8259-5 to service the next interrupt.

Two types of command words are required from the processor to fully define the operating modes of the μPD8259-5.

1. **Initialization Command Words (ICWs)**

   Each μPD8259-5 in the interrupt array must be initialized prior to normal operation. The initialization is performed by a 2 or 3-byte sequence clocked by $\overline{\text{WR}}$ pulses. Figure 1 shows this sequence. (Refer to Figure 2 for bit definitions.)



INITIALIZATION SEQUENCE – FIGURE 1.

2. **Operation Command Words (OCWs)**

The operation command words are used to program the various interrupt algorithms listed below:

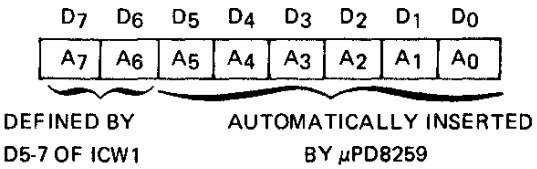
- Fully Nested Mode
- Rotating Priority Mode
- Special Mask Mode
- Polled Mode

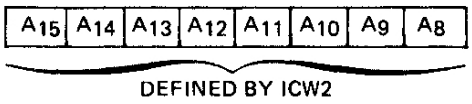
Once the μPD8259-5 has been initialized, OCWs can be written at any time.

When $A_0 = 0$ and $D_4 = 1$ in a command to the μPD8259-5, together with CS = 0, it is recognized as Initialization Command Word 1. This is the start of the initialization sequence and causes the following to occur:

- The Interrupt Request edge-sense circuitry is reset so that an input must make a low-to-high transition to generate its interrupt.
- The initialization sequence clears Interrupt Mask Register to all unmasked and resets the Special Mask Mode and Status Read Flip-Flops.
- IR_7 input is set to priority 7.

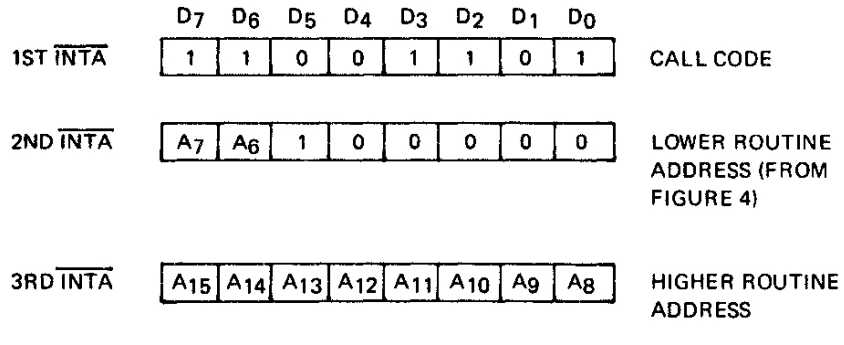
There are eight equally-spaced base vector addresses in memory for the eight interrupt inputs. The interval between the base vector addresses can be programmed to be either four or eight requiring 32 or 64 bytes in memory, respectively. The following shows how the address format is mapped onto the Data bus.





The μPD8259-5 automatically defines A_{0-4} with a separate address for each interrupt input. The base vector addresses A_{15-6} are programmed by ICW1 and ICW2. A_5 is either defined by the μPD8259-5 if the address interval is eight or must be user-define the interval is 4. The 8-byte CALL interval is consistent with 8080A processor RESTART instruction software. The 4-byte CALL interval can be used for a compact jump table. Refer to Figure 4 for a table of address formats.

The following is an example of an interrupt acknowledge sequence. The μPD8259-5 has been programmed for a CALL address (base vector address) interval of eight (F = 0) and there is an interrupt appearing on IR_4. The 3-byte sequence is strobed out to the Data bus by three $\overline{INTA}$ pulses.



It is only necessary to program ICW3 when there are multiple μPD8259-5's in the interrupt array, i.e., S = 0. There are two types of ICW3s. The first is for programming the master μPD8259-5. The second is for the slaves.

1. ICW3-Master μPD8259-5. A "1" is set in S_{0-7} for each corresponding slave in the interrupt array. The S_{0-7} bits, together with $\overline{SP}$ = 1, instructs the cascade buffer/comparator to send the ID of the interrupting slave on the CAS0,1,2 lines.
2. ICW3-SLAVE μPD8259-5(s). Bits D_7-D_3 are "don't care" bits and have no effect on ICW3. The ID of each slave is programmed by bits D_{0-2} ($ID_{0,1,2}$). Once the master μPD8259-5 has sent out the first byte of the CALL sequence, the slave device(s) with their $\overline{SP}$ inputs set to Logic 0, compare their IDs appearing on the CAS0,1,2 lines through the cascade buffer/comparator. The slave whose ID matches the CAS0,1,2 code then issues bytes 2 and 3 of the CALL sequence.

Once the μPD8259-5 has been programmed with Initialization Command Words, it can now be programmed for the appropriate interrupt algorithm by the Operation Command Words. Interrupt algorithms in the μPD8259-5 can be changed at any time during program operation by issuing another set of Operation Command Words. The following sections describe the various algorithms available and their associated OCWs.

INTERRUPT MASKS

The individual Interrupt Request input lines are maskable by setting the corresponding bits in the Interrupt Mask Register to a logic "1" through OCW1. The actual masking is performed upon the contents of the In-Service Register (e.g., if Interrupt Request line 3 is to be masked, then only bit 3 of the IMR is set to logic "1." The IMR in turn acts upon the contents of the ISR to mask bit 3). Once the μPD8259-5 has acknowledged an interrupt, i.e., the μPD8259-5 has sent an INT signal to the processor and the system controller has sent it an $\overline{INTA}$ signal, the interrupt input, although it is masked, will inhibit lower priority requests from being acknowledged. There are two means of enabling these lower priority interrupt lines. The first is by issuing an End-of-Interrupt (EOI) through Operation Command Word 2 (OCW2), thereby resetting the appropriate ISR bit. The second approach is to select the Special Mask Mode through OCW3. The Special Mask Mode (SMM) and End-of-Interrupt (EOI) will be described in more detail further on.

FULLY NESTED MODE

The fully nested mode is the μPD8259-5's basic operating mode. It will operate in this mode after the initialization sequence, requiring no Operation Command Words for formatting. Priorities are set IR_0 through IR_7 with IR_0 the highest priority. After the interrupt has been acknowledged by the processor and system controller, only higher priorities will be serviced. Upon receiving an $\overline{INTA}$, the priority resolver determines the priority of the interrupt, the corresponding ISR bit is set, and the vector address is output to the Data bus. The EOI command resets the corresponding ISR bit at the end of its service routine.

Notes: ① Reference Figure 2
② Reference Figure 3

ROTATING PRIORITY MODE COMMANDS

The two variations of Rotating Priorities are the Auto Rotate and Specific Rotate modes. These two modes are typically used to service interrupting devices of equivalent priorities.

1. Auto Rotate Mode

   Programming the Auto Rotate Mode through OCW2 assigns priorities 0-7 to the interrupt request input lines. Interrupt line IR_0 is set to the highest priority and IR_7 to the lowest. Once an interrupt has been serviced it is automatically assigned the lowest priority. That same input must then wait for the devices ahead of it to be serviced before it can be acknowledged again. The Auto Rotate Mode is selected by programming OCW2 in the following way (refer to Figure 3): set Rotate Priority bit "R" to a logic "1"; program EOI to a logic "1" and SEOI to a logic "0." The EOI and SEOI commands are discussed further on. The following is an example of the Auto Rotate Mode with devices requesting interrupts on lines IR_2 and IR_5.

   Before Interrupts are Serviced:

	IS_7	IS_6	IS_5	IS_4	IS_3	IS_2	IS_1	IS_0
In-Service Register	0	0	1	0	0	1	0	0

Highest Priority →

	IR_7	IR_6	IR_5	IR_4	IR_3	IR_2	IR_1	IR_0
Priority Status Register								

   According to the Priority Status Register, IR_2 has a higher priority than IR_5 and will be serviced first.

   After Servicing:

	IS_7	IS_6	IS_5	IS_4	IS_3	IS_2	IS_1	IS_0
In-Service Register	0	0	1	0	0	0	0	0

Highest Priority →

	IR_2	IR_1	IR_0	IR_7	IR_6	IR_5	IR_4	IR_3
Priority Status Register								

   At the completion of IR_2's service routine the corresponding In-Service Register bit, IS_2 is reset to "0" by the preprogrammed EOI command. IR_2 is then assigned the lowest priority level in the Priority Status Register. The μPD8259-5 is now ready to service the next highest interrupt, which in this case, is IR_5.

2. Specific Rotate Mode

   The priorities are set by programming the lowest level through OCW2. The μPD8259-5 then automatically assigns the highest priority. If, for example, IR_3 is set to the lowest priority (bits L_2, L_1, L_0 form the binary code of the bottom priority level), then IR_4 will be set to the highest priority. The Specific Rotate Mode is selected by programming OCW2 in the following manner: set Rotate Priority bit "R" to a logic "1," program EOI to a logic "0," SEOI to a logic "1" and L_2, L_1, L_0 to the lowest priority level. If EOI is set to a logic "1," the ISR bit defined by L_2, L_1, L_0 is reset.

END-OF-INTERRUPT (EOI) AND SPECIFIC END-OF-INTERRUPT (SEOI)

The End-of-Interrupt or Specific End-of-Interrupt command must be issued to reset the appropriate In-Service Register bit before the completion of a service routine. Once the ISR bit has been reset to logic "0," the μPD8259-5 is ready to service the next interrupt

Two types of EOIs are available to clear the appropriate ISR bit depending on the μPD8259-5's operating mode.

1. Non-Specific End-of-Interrupt (EOI)

   When operating in interrupt modes where the priority order of the interrupt inputs is preserved (e.g., fully nested mode), the particular ISR bit to be reset at the completion of the service routine can be determined. A non-specific EOI command will automatically reset the highest priority ISR bit of those set. The highest priority ISR bit must necessarily be the interrupt being serviced and must necessarily be the service subroutine returned from.

2. Specific End-of-Interrupt (SEOI)

   When operating in interrupt modes where the priority order of the interrupt inputs is not preserved (e.g., rotating priority mode) the last serviced interrupt level may not be known. In these modes a Specific End-of-Interrupt must be issued to clear the ISR bit at the completion of the interrupt service routine. The SEOI is programmed by setting the appropriate bits in OCW3 (Figure 2) to logic "1"s. Both the EOI and SEOI bits of OCW3 must be set to a logic "1" with L_2, L_1, L_0 forming the binary code of the ISR bit to be reset.

SPECIAL MASK MODE

Setting up an interrupt mask through the Interrupt Mask Register (refer to Interrupt Mask Register section) by setting the appropriate bits in OCW1 to a logic "1" will inhibit lower priority interrupts from being acknowledged. In applications requiring that the lower priorities be enabled while the IMR is set, the Special Mask Mode can be used. The SMM is programmed in OCW3 by setting the appropriate bits to a logic "1." Once the SMM is set, the μPD8259-5 remains in this mode until it is reset. The Special Mask Mode does not affect the higher priority interrupts.

POLLED MODE

In the Poll Mode the processor must be instructed to disable its interrupt input (INT). Interrupt service is initiated through software by a Poll Command. The Poll Mode is programmed by setting the Poll Mode bit in OCW3 (P = 1), during a $\overline{WR}$ pulse. The following $\overline{RD}$ pulse is then considered as an interrupt acknowledge. If an interrupt input is present, that $\overline{RD}$ pulse sets the appropriate ISR bit and reads the interrupt priority level. The Poll Mode is a one-time operation and must be programmed through OCW3 before every read. The word strobed onto the Data bus during Poll Mode is of the form:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
I	X	X	X	X	W_2	W_1	W_0

where: I = 1 if there is an interrupt requesting service
= 0 if there are no interrupts

$W_{2\text{-}0}$ forms the binary code of the highest priority level of the interrupts requesting service

The Poll Mode can be used when an interrupt service routine is common to several interrupt inputs. The $\overline{INTA}$ sequence is no longer required offering a saving in ROM space. The Poll Mode can also be used to expand the number of interrupts beyond 64.

The following major registers' status is available to the processor by appropriately formatting OCW3 and issuing $\overline{RD}$ command.

INTERRUPT REQUEST REGISTER (8-BITS)

The Interrupt Request Register stores the interrupt levels awaiting acknowledgement. Once it has been acknowledged, the highest priority in-service bit is reset. (Note that the Interrupt Mask Register has no effect on the IRR.) A $\overline{WR}$ command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. The bits which determine whether the IRR and ISR are being read from are RIS and ERIS. To read contents of the IRR, ERIS must be logic "1" and RIS a logic "0."

IN-SERVICE REGISTER (8-BITS)

The In-Service Register stores the priorities of the interrupt levels being serviced. Assertion of an End-of-Interrupt (EOI) updates the ISR to the next priority level. A $\overline{WR}$ command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. Both ERIS and RIS should be set to a logic "1."

INTERRUPT MASK REGISTER (8-BITS)

The Interrupt Mask Register holds mask data modifying interrupt levels. To read the IMR status a $\overline{WR}$ pulse preceding the $\overline{RD}$ is not necessary. The IMR data is available to the data bus when $\overline{RD}$ is asserted with A_0 at a logic "1."

A single OCW3 is sufficient to enable successive status reads providing it is of the same register. A status read is over-ridden by the Poll Mode where bits P and ERIS of OCW3 are set to a logic "1."

If more than eight interrupt levels are required, multiple μPD8259-5's can be cascaded with one master and up to eight slaves, to accommodate up to 64 levels of interrupt.

As shown in Figure 5, the master device directs the appropriate slave to release its CALL address through its three cascade lines (CAS0,1,2).

The INT output of the slave devices go to the IR inputs of the master device. The master μPD8259-5's INT output is connected to the processor's control bus. When the slave device signals the master that it has acknowledged an interrupt, the master issues an 8080A CALL Op-code at the first $\overline{INTA}$ pulse. The master then signals that slave device (via CAS0,1,2) to issue the appropriate CALL address during the second and third $\overline{INTA}$ pulses.

The slave address code is present on cascade lines 0,1,2 (active-high logic) from the trailing edge of the first $\overline{INTA}$ to the trailing edge of the third $\overline{INTA}$. Each device in the μPD8259-5 array must be individually initialized and can be programmed in different operating modes. Two End-of-Interrupt commands must be issued for the master and its corresponding slave. An address decoder is used to drive the Chip Select inputs for each μPD8259-5 in the array. The Slave Program ($\overline{SP}$) input must be held at a logic " "0" level for each slave device and held at logic "1" level for the master. The SP input selects the Cascade lines as either inputs (SP = 0) or outputs (SP = 1).

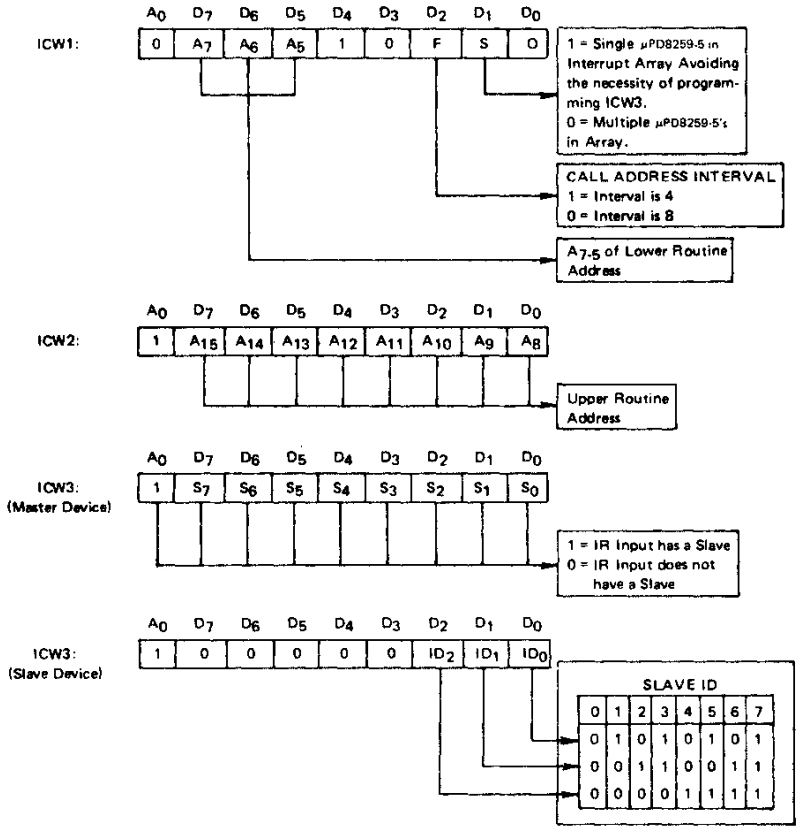


FIGURE 2

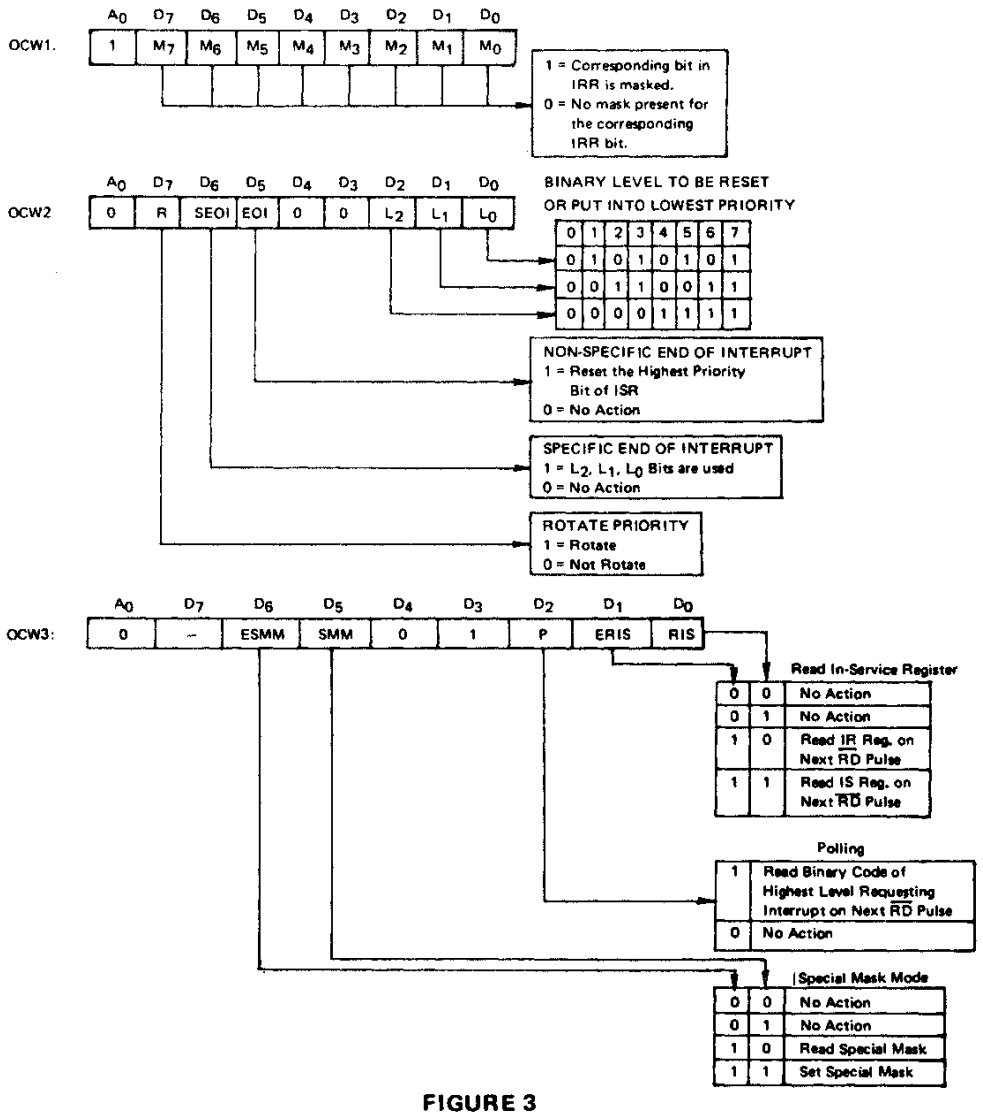


FIGURE 3

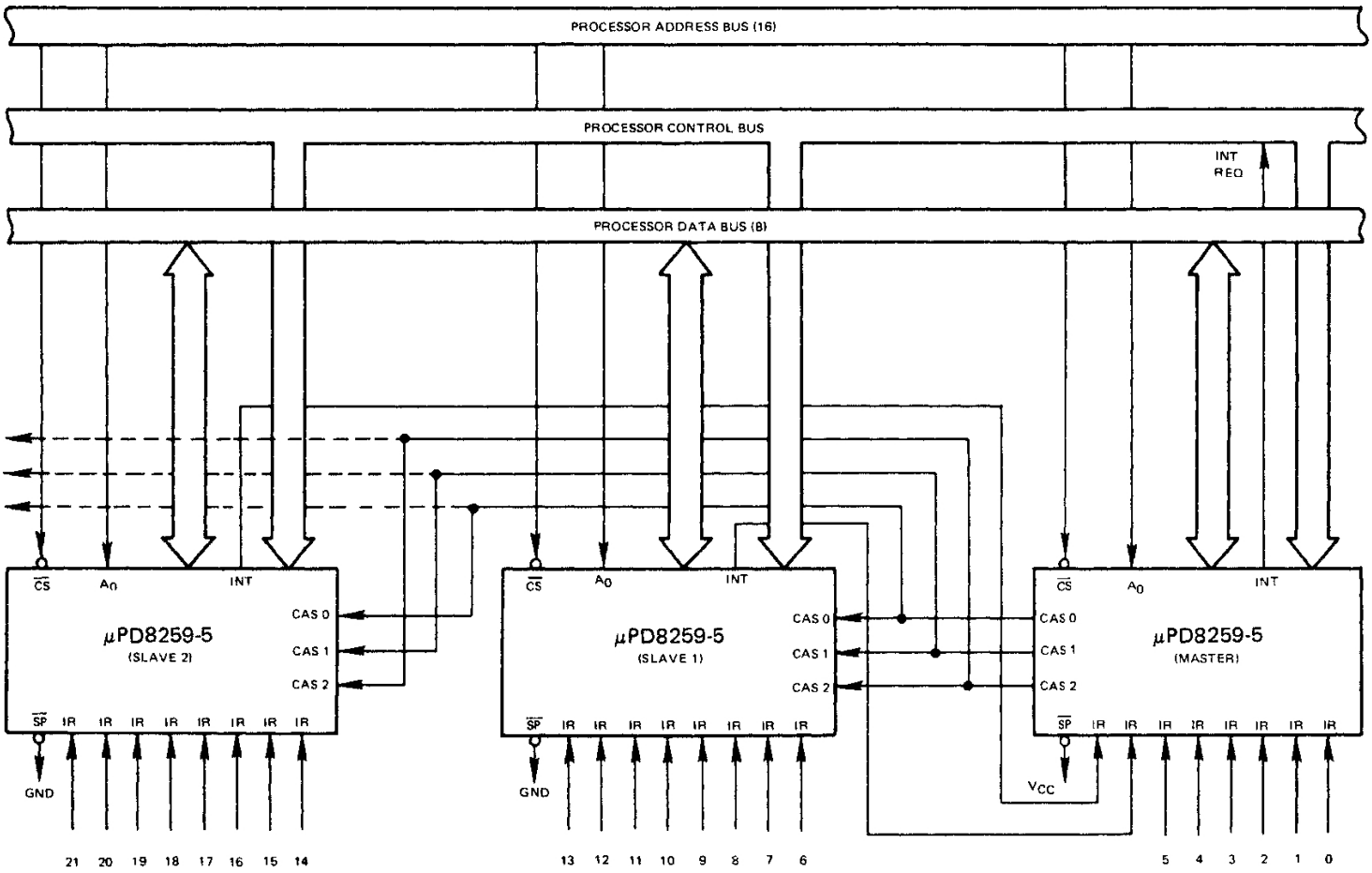
	A_0	D_4	D_3				
OCW1	1	X	X	M_7-M_0			IMR (Interrupt Mask Register) $\overline{WR}$ loads IMR data while $\overline{RD}$ reads status
OCW2	0	0	0	R	SEOI	EOI	
				0	0	0	No Action
				0	0	1	Non-Specific End-of-Interrupt
				0	1	0	No Action
				0	1	1	Specific-End-of-Interrupt L_2, L_1, L_0 forms binary representation of level to be reset.
				1	0	0	No Action
				1	0	1	Rotate Priority at End-of-Interrupt (Auto Mode)
				1	1	0	Rotate Priority, L_2, L_1, L_0 specifies bottom priority without End-of-Interrupt
				1	1	1	Rotate Priority at End-of-Interrupt (Specific Mode). L_2, L_1, L_0 specifies bottom priority, and its In-Service Register bit is reset.
OCW3	0	0	1	ESMM	SMM		
				0	0		Special Mask not affected
				0	1		
				1	0		Reset Special Mask
				1	1		Set Special Mask
				ERIS	RIS		
				0	0		No Action
				0	1		
				1	0		Read IR Register Status
				1	1		Read IS Register Status

	INTERVAL = 4								INTERVAL = 8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_7	A_7	A_6	A_5	1	1	1	0	0	A_7	A_6	1	1	1	0	0	0
IR_6	A_7	A_6	A_5	1	1	0	0	0	A_7	A_6	1	1	0	0	0	0
IR_5	A_7	A_6	A_5	1	0	1	0	0	A_7	A_6	1	0	1	0	0	0
IR_4	A_7	A_6	A_5	1	0	0	0	0	A_7	A_6	1	0	0	0	0	0
IR_3	A_7	A_6	A_5	0	1	1	0	0	A_7	A_6	0	1	1	0	0	0
IR_2	A_7	A_6	A_5	0	1	0	0	0	A_7	A_6	0	1	0	0	0	0
IR_1	A_7	A_6	A_5	0	0	1	0	0	A_7	A_6	0	0	1	0	0	0
IR_0	A_7	A_6	A_5	0	0	0	0	0	A_7	A_6	0	0	0	0	0	0

FIGURE 4

Note: Insure that the processor's interrupt input is disabled during the execution of any control command and initialization sequence for all μPD8259-5's.

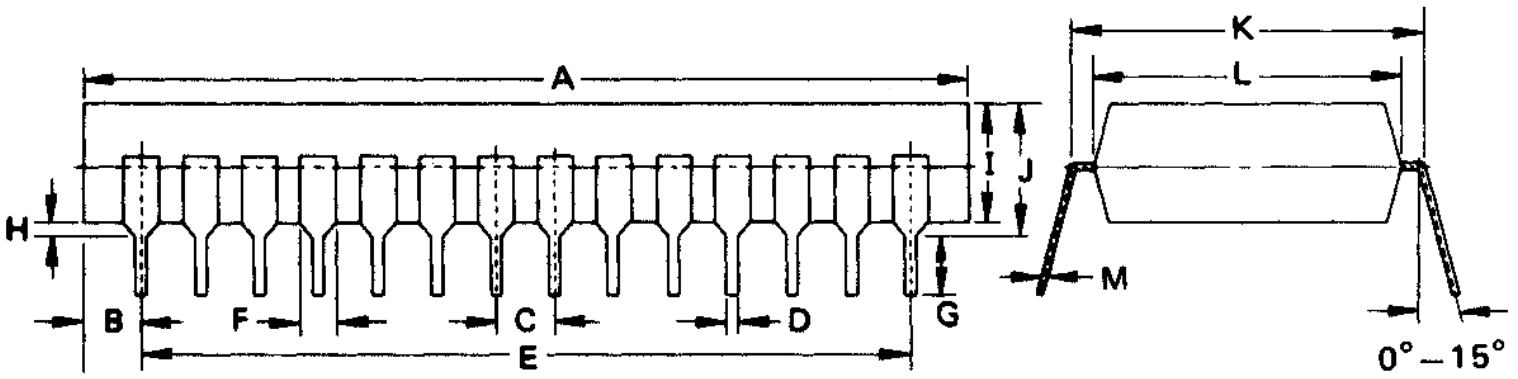
CASCADING THE μPD8259-5



INSTRUCTION SET

Instruction Number	Mnemonic	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operation Description
1	ICW1 A	0	A_7	A_6	A_5	1	0	1	1	0	Byte 1 Initialization, Format = 4, Single
2	ICW1 B	0	A_7	A_6	A_5	1	0	1	0	0	Byte 1 Initialization, Format = 4, Not Single
3	ICW1 C	0	A_7	A_6	A_5	1	0	0	1	0	Byte 1 Initialization, Format = 8, Single
4	ICW1 D	0	A_7	A_6	A_5	1	0	0	0	0	Byte 1 Initialization, Format = 8, Not Single
5	ICW2	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	Byte 2 Initialization (Address No. 2)
6	ICW3 M	1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	Byte 2 Initialization — MASTER
7	ICW3 S	1	0	0	0	0	0	S_2	S_1	S_0	Byte 3 Initialization — SLAVE
8	OCW1	1	M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0	Load Mask Register, Read Mask Register
9	OCW2 E	0	0	0	1	0	0	0	0	0	Non-Specific EOI
10	OCW2 SE	0	0	1	1	0	0	L_2	L_1	L_0	Specific EOI, L_2, L_1, L_0 Code of IS to be Reset
11	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate at EOI (Auto Mode)
12	OCW2 RSE	0	1	1	1	0	0	L_2	L_1	L_0	Rotate at EOI (Specific Mode). L_2, L_1, L_0 Code of Line to be Reset and Selected as Bottom Priority.
13	OCW2 RS	0	1	1	0	0	0	L_2	L_1	L_0	L_2, L_1, L_0 — Code of Bottom Priority Line.
14	OCW3 P	0	—	0	0	0	1	1	0	0	Poll Mode
15	OCW3 RIS	0	—	0	0	0	1	0	1	1	Read IS Register
16	OCW3 RR	0	—	0	0	0	1	0	1	0	Read Requests Register
17	OCW3 SM	0	—	1	1	0	1	0	0	0	Set Special Mask Mode
18	OCW3 RSM	0	—	1	0	0	1	0	0	0	Reset Special Mask Mode

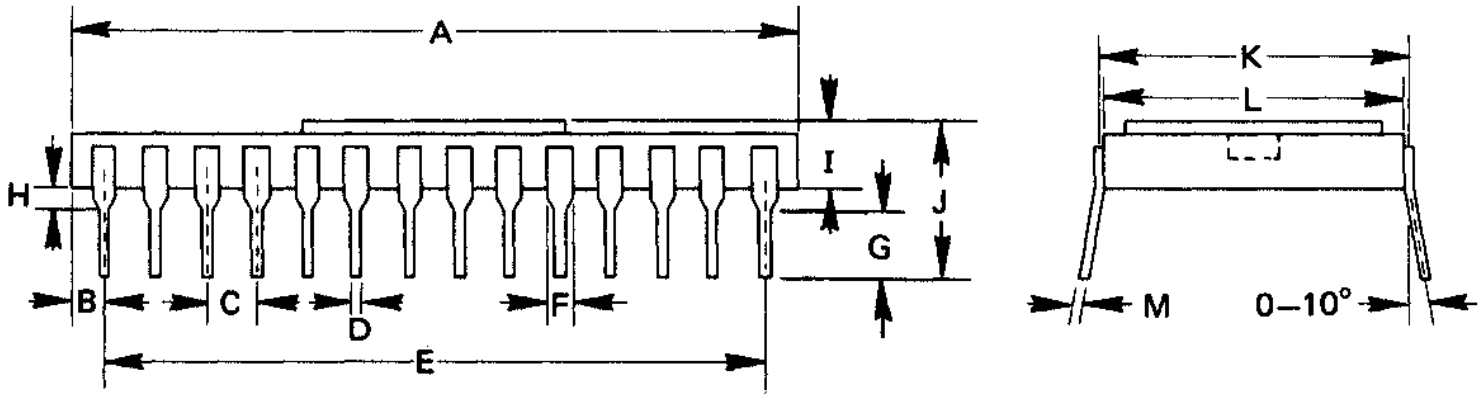
Note: Insure that the processor's interrupt input is disabled during the execution of any control command and initialization sequence for all μPD8259-5's.



(Plastic)

μPD8259-5C

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$



(Ceramic)

μPD8259-5D

ITEM	MILLIMETERS	INCHES
A	36.2 MAX.	1.43 MAX.
B	1.59 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.46 ± 0.01	0.02 ± 0.004
E	33.02 ± 0.1	1.3 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.002