NEC Microcomputers, Inc.

NEC

μPD8086
μPD8086-2*

16 BIT MICROPROCESSOR

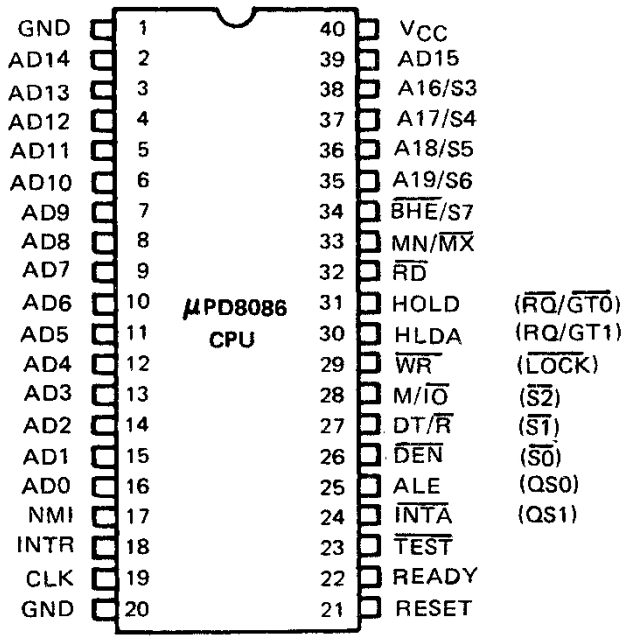
DESCRIPTION

The μPD8086 is a 16-bit microprocessor that has both 8-bit and 16-bit attributes. It has a 16-bit wide physical path to memory for high performance. Its architecture allows higher throughput than the 5 MHz μPD8085A-2.

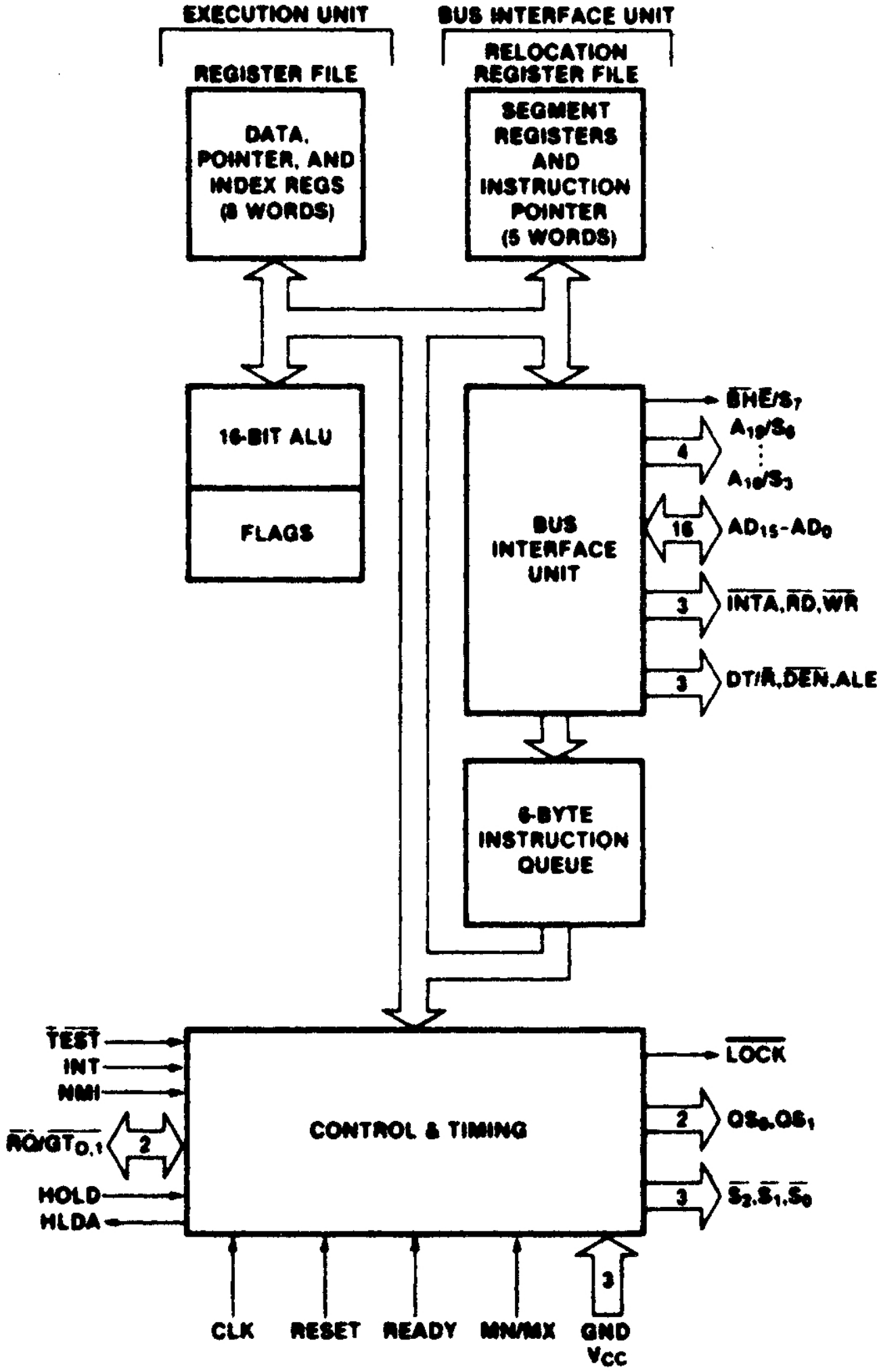
FEATURES

- Can Directly Address 1 Megabyte of Memory
- Fourteen 16-Bit Registers with Symmetrical Operations
- Bit, Byte, Word, and Block Operations
- 8 and 16-Bit Signed and Unsigned Arithmetic Operations in Binary or Decimal
- Multiply and Divide Instructions
- 24 Operand Addressing Modes
- Assembly Language Compatible with the μPD8080/8085
- Complete Family of Components for Design Flexibility

PIN CONFIGURATION



NO.	SYMBOL	NAME	FUNCTION
2-16, 39	AD0-AD15	Address/Data Bus	Multiplexed address (T_1) and data (T_2, T_3, T_W, T_4) bus. 8-bit peripherals tied to the lower 8 bits, use A0 to condition chip select functions. These lines are tri-state during interrupt acknowledge and hold states.
17	NMI	Non-Maskable Interrupt	This is an edge triggered input causing a type 2 interrupt. A look-up table is used by the processor for vectoring information.
18	INTR	Interrupt Request	A level triggered input sampled on the last clock cycle of each instruction. Vectoring is via an interrupt look-up table. INTR can mask in software by resetting the interrupt enable bit.
19	CLK	Clock	The clock input is a 1/3 duty cycle input basic timing for the processor and bus controller.
21	RESET	Reset	This active high signal must be high for 4 clock cycles. When it returns low, the processor restarts execution.
22	READY	Ready	An acknowledgement from memory or I/O that data will be transferred. Synchronization is done by the μPD8284 clock generator.
23	$\overline{TEST}$	Test	This input is examined by the "WAIT" instruction, and if low, execution continues. Otherwise the processor waits in an "Idle" state. Synchronized by the processor on the leading edge of CLK.
24	$\overline{INTA}$	Interrupt Acknowledge	This is a read strobe for reading vectoring information. During T_2, T_3, and T_W of each interrupt acknowledge cycle it is low.
25	$\overline{ALE}$	Address Latch Enable	This is used in conjunction with the μPD8282/8283 latches to latch the address, during T_1 of any bus cycle.
26	$\overline{DEN}$	Data Enable	This is the output enable for the μPD8282/8287 transceivers. It is active low during each memory and I/O access and INTA cycles.
27	DT/$\overline{R}$	Data Transmit/Receive	Used to control the direction of data flow through the transceivers.
28	M/$\overline{IO}$	Memory/IO Status	This is used to separate memory access from I/O access.
29	$\overline{WR}$	Write	Depending on the state of the M/$\overline{IO}$ line, the processor is either writing to I/O or memory.
30	HLDA	Hold Acknowledge	A response to the HOLD input, causing the processor to tri-state the local bus. The bus return active one cycle after HOLD goes back low.
31	HOLD	Hold	When another device requests the local bus, driving HOLD high, will cause the μPD8086 to issue a HLDA.
32	$\overline{RD}$	Read	Depending on the state of the M/$\overline{IO}$ line, the processor is reading from either memory or I/O.
33	MN/$\overline{MX}$	Minimum/Maximum	This input is to tell the processor which mode it is to be used in. This effects some of the pin descriptions.
34	$\overline{BHE}$/S_7	Bus/High Enable	This is used in conjunction with the most significant half of the data bus. Peripheral devices on this half of the bus use BHE to condition chip select functions.
35-38	A16-A19	Most Significant Address Bits	The four most significant address bits for memory operations. Low during I/O operations.
26, 27, 28 34-38	S_0-S_7	Status Outputs	These are the status outputs from the processor. They are used by the μPD8288 to generate bus control signals.
24, 25	QS_1, QS_0	Que Status	Used to track the internal μPD8086 instruction que.
29	$\overline{LOCK}$	Lock	This output is set by the "LOCK" instruction to prevent other system bus masters from gaining control.
30, 31	$\overline{RQ}$/GT_0 $\overline{RQ}$/GT_1	Request/Grant	Other local bus masters can force the processor to rebase the local bus at the end of the current bus cycle.


EXECUTION UNIT
BUS INTERFACE UNIT
REGISTER FILE
RELOCATION REGISTER FILE
DATA, POINTER, AND INDEX REGS (8 WORDS)
SEGMENT REGISTERS AND INSTRUCTION POINTER (5 WORDS)
16-BIT ALU
FLAGS
BUS INTERFACE UNIT
6-BYTE INSTRUCTION QUEUE
CONTROL & TIMING
BHE/S7
A19/S6
A16/S3
AD15-AD0
INTA, RD, WR
DT/R, DEN, ALE
TEST
INT
NMI
RQ/GT0,1
HOLD
HLDA
LOCK
QS0, QS1
S2, S1, S0
CLK
RESET
READY
MN/MX
GND
Vcc
4
16
3
2

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . −1.0 to +7V
Power Dissipation 2.5W

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

T_a = 0°C to 70°C; V_{CC} = 5V ± 10%

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5	+0.8	V	
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −400 μA
Power Supply Current μPD8086/ μPD8086-2	I_{CC}		 340 350	 mA mA	T_a = 25°C
Input Leakage Current	I_{LI}		±10	μA	$0V < V_{IN} < V_{CC}$
Output Leakage Current	I_{LO}		±10	μA	$0.45V \leqslant V_{OUT} \leqslant V_{CC}$
Clock Input Low Voltage	V_{CL}	−0.5	+0.6	V	
Clock Input High Voltage	V_{CH}	3.9	V_{CC} + 1.0	V	
Capacitance of Input Buffer (All input except AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)	C_{IN}		15	pF	fc = 1 MHz
Capacitance of I/O Buffer (AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)	C_{IO}		15	pF	fc = 1 MHz

TIMING REQUIREMENTS

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
CLK Cycle Period – μPD8086	TCLCL	200	500	125	500	ns	
CLK Low Time	TCLCH	(2/3 TCLCL) –15		(2/3 TCLCL) –15		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2		(1/3 TCLCL) +2		ns	
CLK Rise Time	TCH1CH2		10		10	ns	From 1.0V to 3.5V
CLK Fall Time	TCL2CL1		10		10	ns	From 3.5V to 1.0V
Data In Setup Time	TDVCL	30		20		ns	
Data In Hold Time	TCLDX	10		10		ns	
RDY Setup Time into μPD8284 ① ②	TR1VCL	35		35		ns	
RDY Hold Time into μPD8284 ① ②	TCLR1X	0		0		ns	
READY Setup Time into μPD8086	TRYHCH	(2/3 TCLCL) –15		(2/3 TCLCL) –15		ns	
READY Hold Time into μPD8086	TCHRYX	30		20		ns	
READY Inactive to CLK ③	TRYLCL	–8		–8		ns	
HOLD Setup Time	THVCH	35		20		ns	
INTR, NMI, $\overline{\text{TEST}}$ Setup Time ②	TINVCH	30		15		ns	

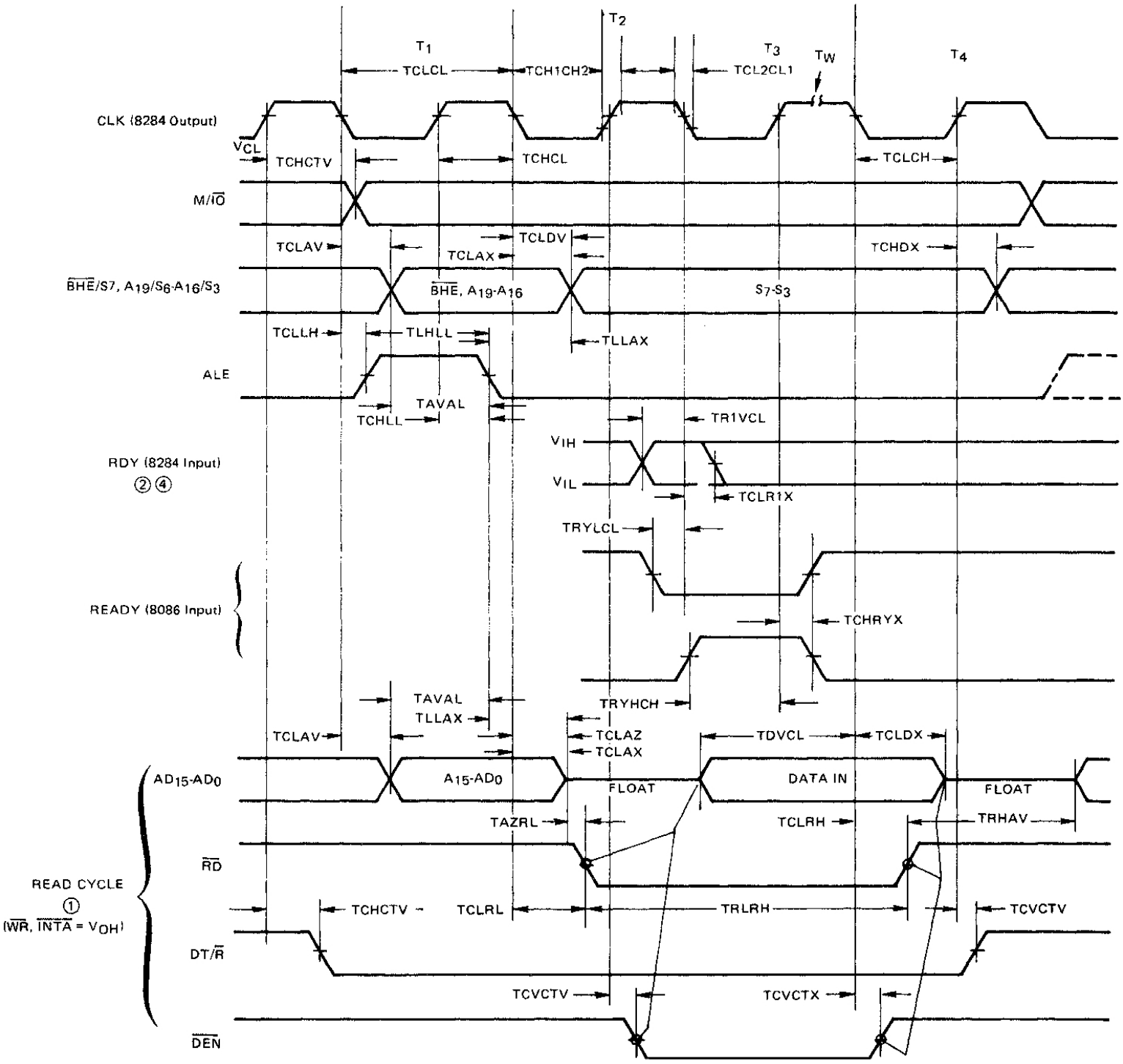
TIMING RESPONSES

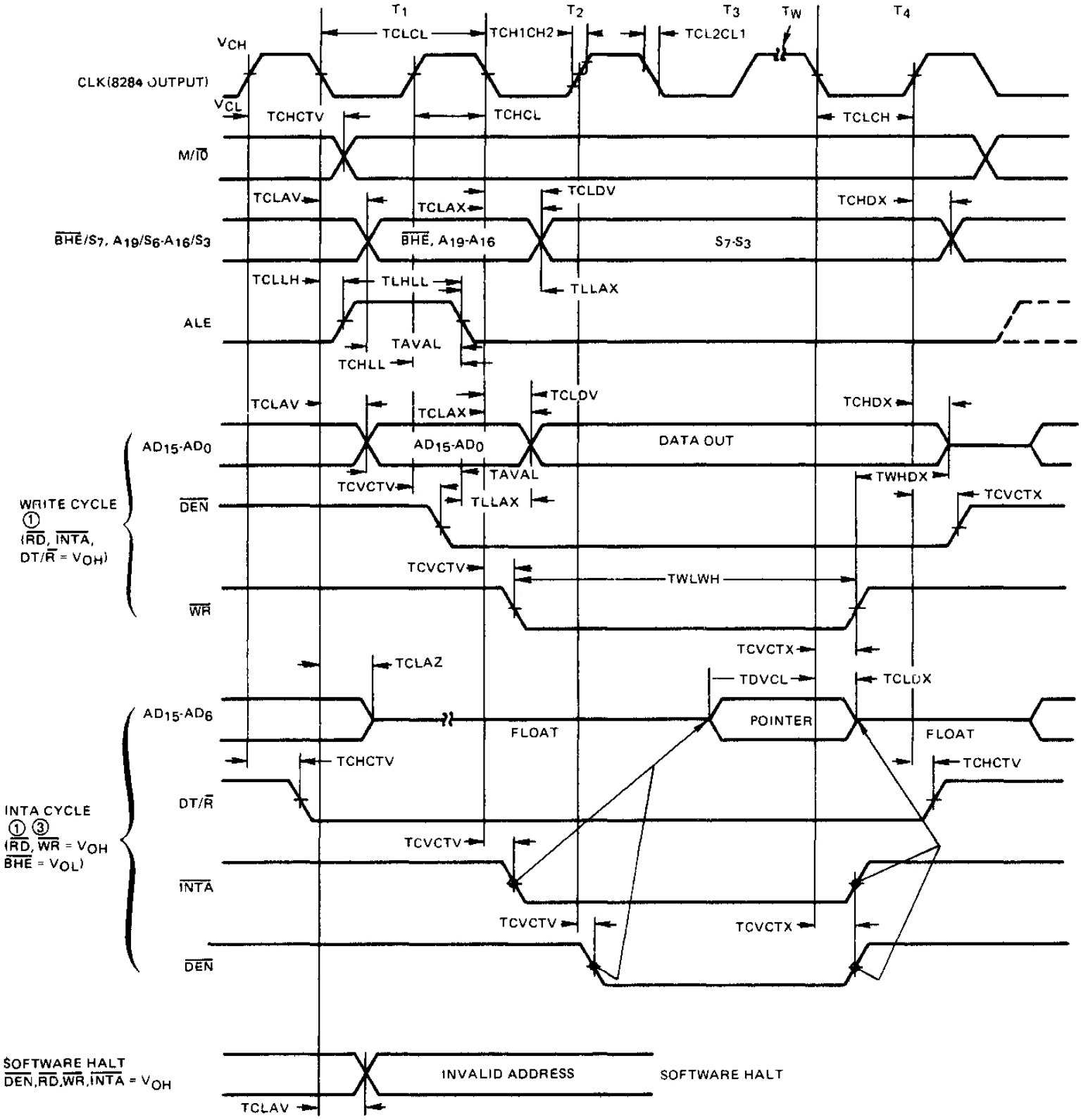
PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Address Valid Delay	TCLAV	10	110	10	60		C_L = 20-100 pF for all μPD8086 Outputs (In addition to μPD8086 self-load)
Address Hold Time	TCLAX	10		10		ns	
Address Float Delay	TCLAZ	TCLAX	80	TCLAX	50	ns	
ALE Width	TLHLL	TCLCH–20		TCLCH–10		ns	
ALE Active Delay	TCLLH		80		50	ns	
ALE Inactive Delay	TCHLL		85		55	ns	
Address Hold Time to ALE Inactive	TLLAX	TCHCL–10		TCHCL–10		ns	
Data Valid Delay	TCLDV	10	110	10	60	ns	
Data Hold Time	TCHDX	10		10		ns	
Data Hold Time After WR	TWHDX	TCLCH–30		TCLCH–30		ns	
Control Active Delay 1	TCVCTV	10	110	10	70	ns	
Control Active Delay 2	TCHCTV	10	110	10	60	ns	
Control Active Delay	TCVCTX	10	110	10	70	ns	
Address Float to READ Active	TAZRL	0		0		ns	
$\overline{\text{RD}}$ Active Delay	TCLRL	10	165	10	100	ns	
$\overline{\text{RD}}$ Inactive Delay	TCLRH	10	150	10	80	ns	
$\overline{\text{RD}}$ Inactive to Next Address Active	TRHAV	TCLCL–45		TCLCL–40		ns	
HLDA Valid Delay	TCLHAV	10	160	10	100	ns	
$\overline{\text{RD}}$ Width	TRLRH	2TCLCL–75		2TCLCL–50		ns	
$\overline{\text{WR}}$ Width	TWLWH	2TCLCL–60		2TCLCL–40		ns	
Address Valid to ALE Low	TAVAL	TCLCH–60		TCLCH–40		ns	

NOTES: ① Signal at μPD8284 shown for reference only.

② Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

③ Applies only to T2 state. (8 ns into T3)


T1
T2
T3
TW
T4
TCLCL
TCH1CH2
TCL2CL1
CLK (8284 Output)
VCL
TCHCTV
TCHCL
TCLCH
M/IO
TCLAV
TCLDV
TCLAX
TCHDX
BHE/S7, A19/S6-A16/S3
BHE, A19-A16
S7-S3
TCLLH
TLHLL
TLLAX
ALE
TAVAL
TCHLL
TR1VCL
VIH
VIL
RDY (8284 Input)
2 4
TCLR1X
TRYLCL
READY (8086 Input)
TCHRYX
TRYHCH
TAVAL
TLLAX
TCLAV
TCLAZ
TCLAX
TDVCL
TCLDX
AD15-AD0
A15-AD0
FLOAT
DATA IN
FLOAT
TAZRL
TCLRH
TRHAV
RD
READ CYCLE
1
(WR, INTA = VOH)
TCHCTV
TCLRL
TRLRH
TCVCTV
DT/R
TCVCTV
TCVCTX
DEN



NOTES: ① All signals switch between V_{OH} and V_{OL} unless otherwise specified.

② RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.

③ Two INTA cycles run back-to-back. The μPD8086 local ADDR/Data Bus is floating during both INTA cycles. Control signals shown for second INTA cycle.

④ Signals at μPD8284 are shown for reference only.

⑤ All timing measurements are made at 1.5V unless otherwise noted.

TIMING WITH μPB8288 BUS CONTROLLER

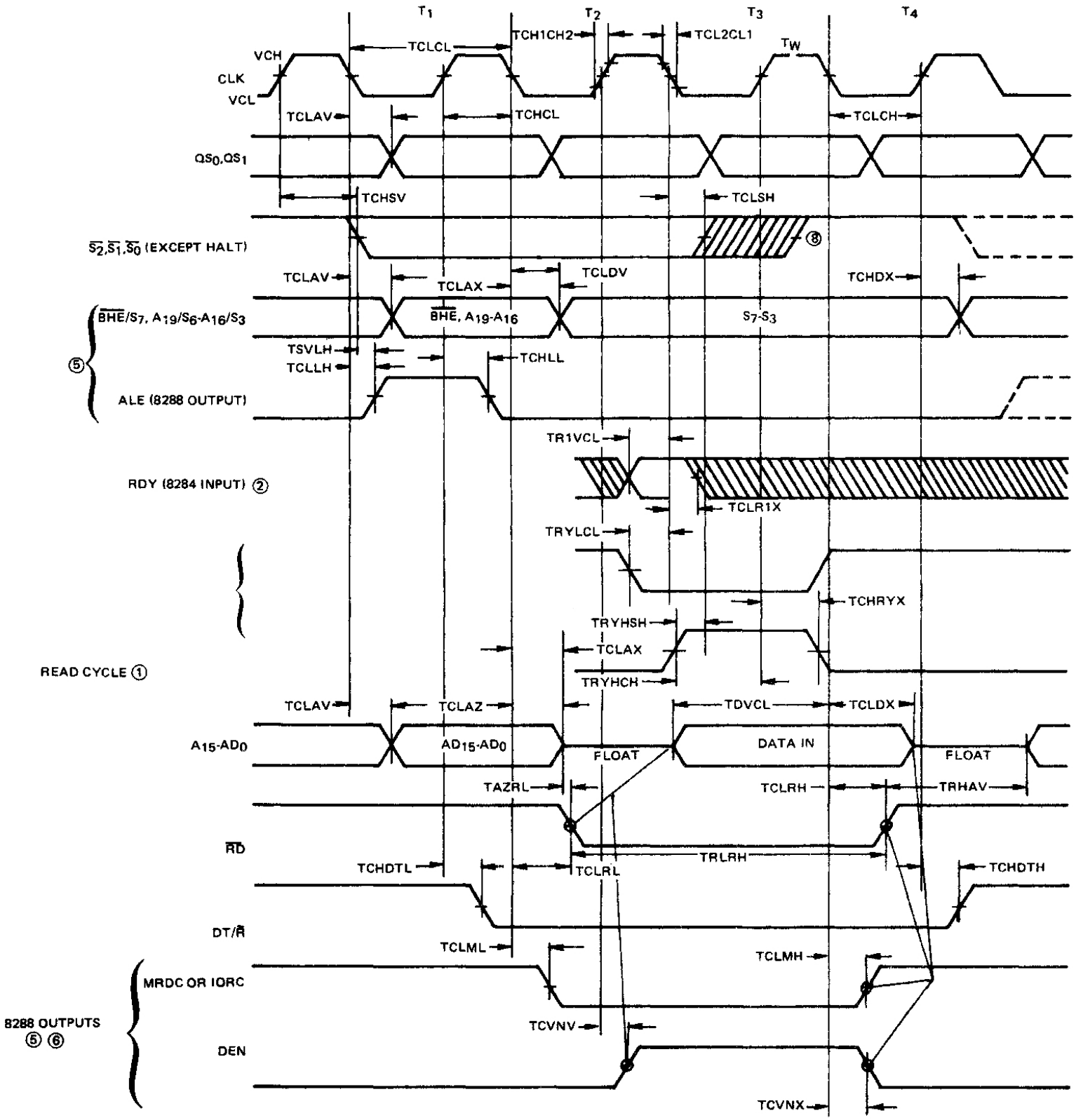
TIMING REQUIREMENTS

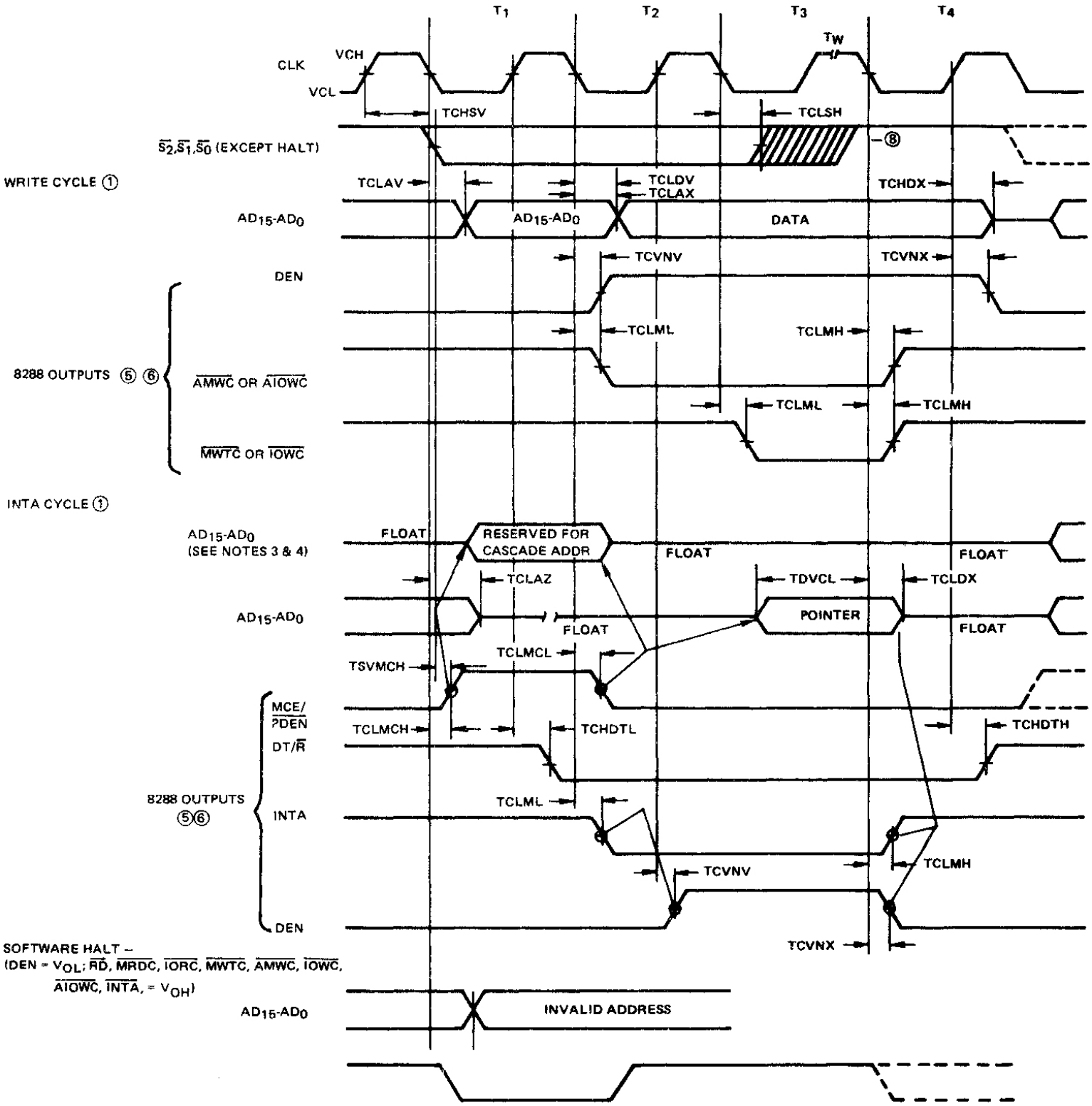
PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
CLK Cycle Period – μPD8086	TCLCL	200	500	125	500	ns	
CLK Low Time	TCLCH	(2/3 TCLCL) -15		(2/3 TCLCL) -15		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2		(1/3 TCLCL) +2		ns	
CLK Rise Time	TCH1CH2		10		10	ns	From 1.0V to 3.5V
CLN Fall Time	TCL2CL1		10		10	ns	From 3.5V to 1.0V
Data in Setup Time	TDVCL	30		20		ns	
Data in Hold Time	TCLDX	10		10		ns	
RDY Setup Time into μPD8284 ① ②	TR1VCL	35		35		ns	
RDY Hold Time into μPD8284 ① . ②	TCLR1X	0		0		ns	
READY Setup Time into μPD8086	TRYHCH	(2/3 TCLCL) -15		(2/3 TCLCL) -15		ns	
READY Hold Time into μPD8086	TCHRYX	30		20		ns	
READY inactive to CLK ④	TRYLCL	-8		-8		ns	
Setup Time for Recognition (INTR, NMI, $\overline{\text{TEST}}$) ②	TINVCH	30		15		ns	
$\overline{\text{RQ}}$/GT Setup Time	TGVCH	30		15		ns	
$\overline{\text{RQ}}$ Hold Time into μPD8086	TCHGX	40		30		ns	

TIMING RESPONSES

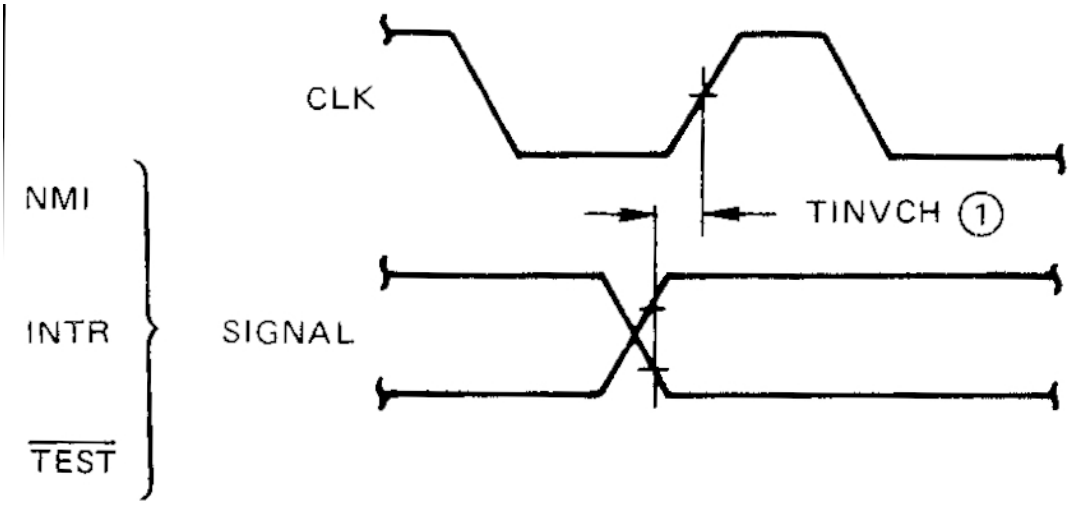
PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Command Active Delay (See Note 1)	TCLML	10	35	10	35	ns	
Command Inactive Delay (See Note 1)	TCLMH	10	35	10	35	ns	
READY Active to Status Passive (See Note 3)	TRYHSH		110		65	ns	
Status Active Delay	TCHSV	10	110	10	60	ns	
Status Inactive Delay	TCLSH	10	130	10	70	ns	
Address Valid Delay	TCLAV	10	110	10	60	ns	
Address Hold Time	TCLAX	10		10		ns	
Address Float Delay	TCLAZ	TCLAX	80	TCLAX	50	ns	
Status Valid to ALE High (See Note 1)	TSVLH		15		15	ns	
Status Valid to MCE High (See Note 1)	TSVMCH		15		15	ns	
CLK Low to ALE Valid (See Note 1)	TCLLH		15		15	ns	
CLK Low to MCE High (See Note 1)	TCLMCH		15		15	ns	
ALE Inactive Delay (See Note 1)	TCHLL		15		15	ns	C_L = 20-100 pF for all μPD8086 Outputs (In addition to μPD8086 self-load)
MCE Inactive Delay (See Note 1)	TCLMCL		15		15	ns	
Data Valid Delay	TCLDV	10	110	10	60	ns	
Data Hold Time	TCHDX	10		10		ns	
Control Active Delay (See Note 1)	TCVNV	5	45	5	45	ns	
Control Inactive Delay (See Note 1)	TCVNX	10	45	10	45	ns	
Address Float to Read Active	TAZRL	0		0		ns	
RD Active Delay	TCLRL	10	165	10	100	ns	
RD Inactive Delay	TCLRH	10	150	10	80	ns	
RD Inactive to Next Address Active	TRHAV	TCLCL-45		TCLCL-40		ns	
Direction Control Active Delay (See Note 1)	TCHDTL		50		50	ns	
Direction Control Inactive Delay (See Note 1)	TCHDTH		30		30	ns	
$\overline{\text{GT}}$ Active Delay	TCLGL	0	85	0	50	ns	
$\overline{\text{GT}}$ Inactive Delay	TCLGH	0	85	0	50	ns	
$\overline{\text{RD}}$ Width	TRLRH	2TCLCL 50		2TCLCL-50		ns	

NOTES: ① Signal at μPB8284 or μPB8288 shown for reference only.
② Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
③ Applies only to T3 and wait states.
④ Applies only to T2 state (8 ns into T3).

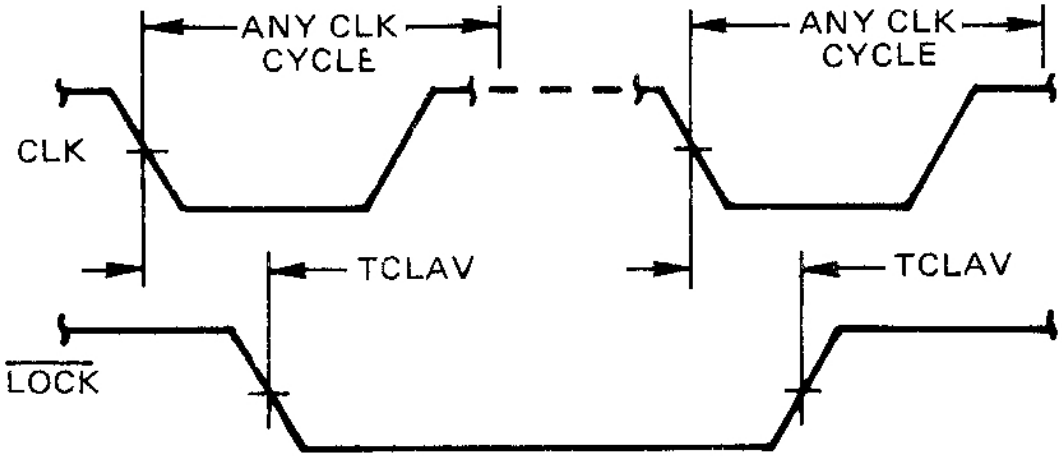

T1
T2
T3
T4
TCLCL
TCH1CH2
TCL2CL1
TW
VCH
CLK
VCL
TCLAV
TCHCL
TCLCH
QS0,QS1
TCHSV
TCLSH
S2,S1,S0 (EXCEPT HALT)
TCLAV
TCLAX
TCLDV
TCHDX
BHE/S7, A19/S6-A16/S3
BHE, A19-A16
S7-S3
TSVLH
TCLLH
TCHLL
ALE (8288 OUTPUT)
TR1VCL
RDY (8284 INPUT) ②
TCLR1X
TRYLCL
TCHRYX
TRYHSH
TCLAX
READ CYCLE ①
TRYHCH
TCLAV
TCLAZ
TDVCL
TCLDX
A15-AD0
AD15-AD0
FLOAT
DATA IN
FLOAT
TAZRL
TCLRH
TRHAV
RD
TRLRH
TCHDTL
TCLRL
TCHDTH
DT/R
TCLML
TCLMH
MRDC OR IORC
8288 OUTPUTS
⑤ ⑥
TCVNV
DEN
TCVNX

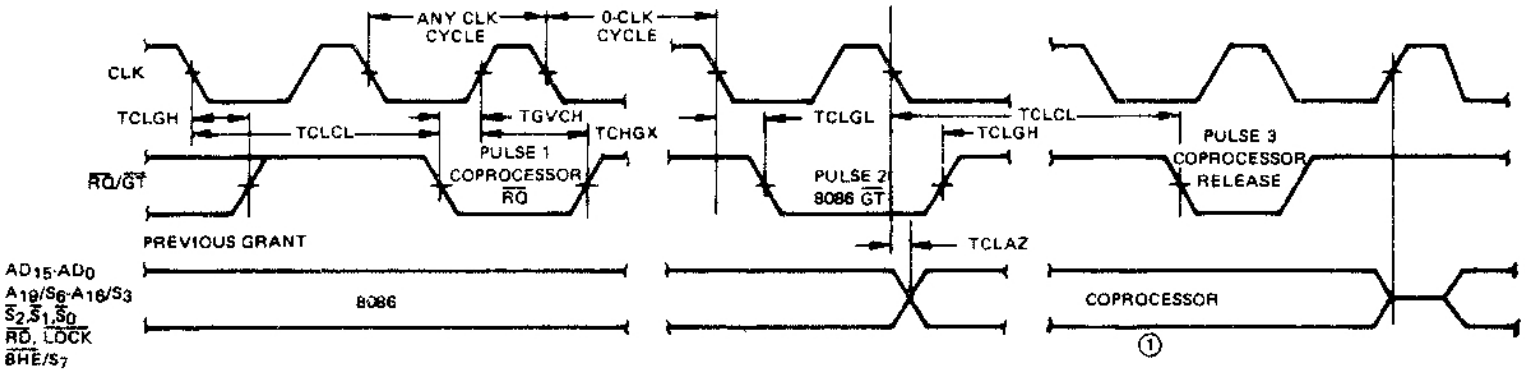


NOTES:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycle.
4. Two INTA cycles run back-to-back. The 8086 local ADDR/Data Bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5. Signals at 8284 or 8288 are shown for reference only.
6. The issuance of the 8288 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high 8288 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T_4.



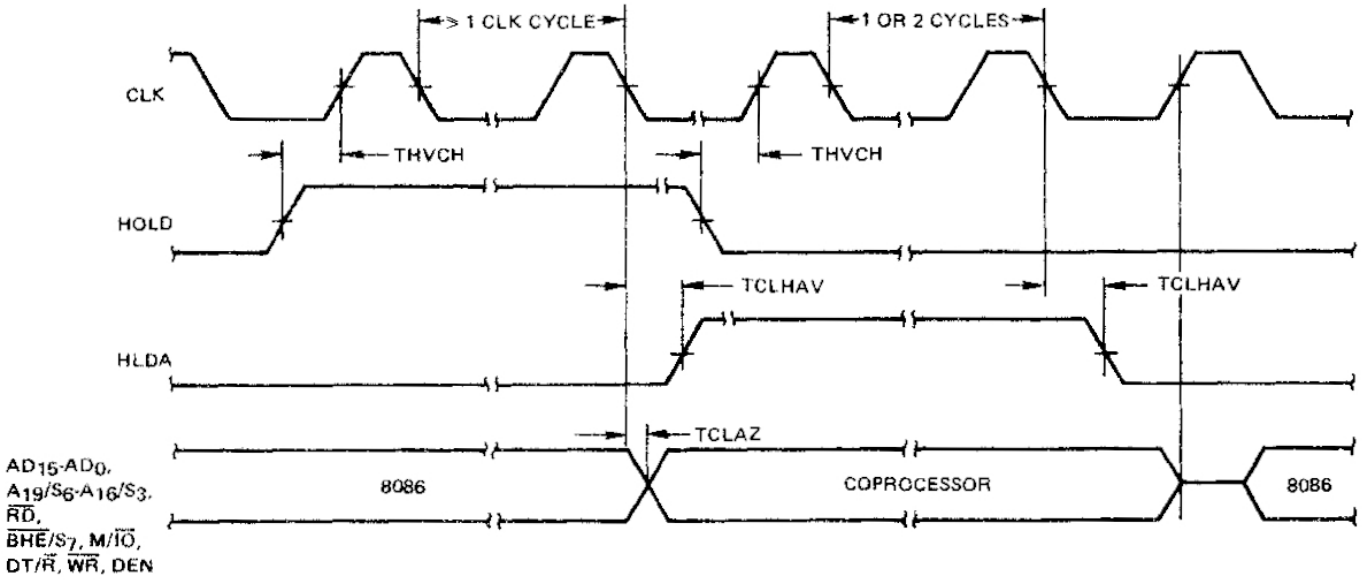
NOTE: (1) Setup requirements for asynchronous signals only to guarantee recognition at next CLK.



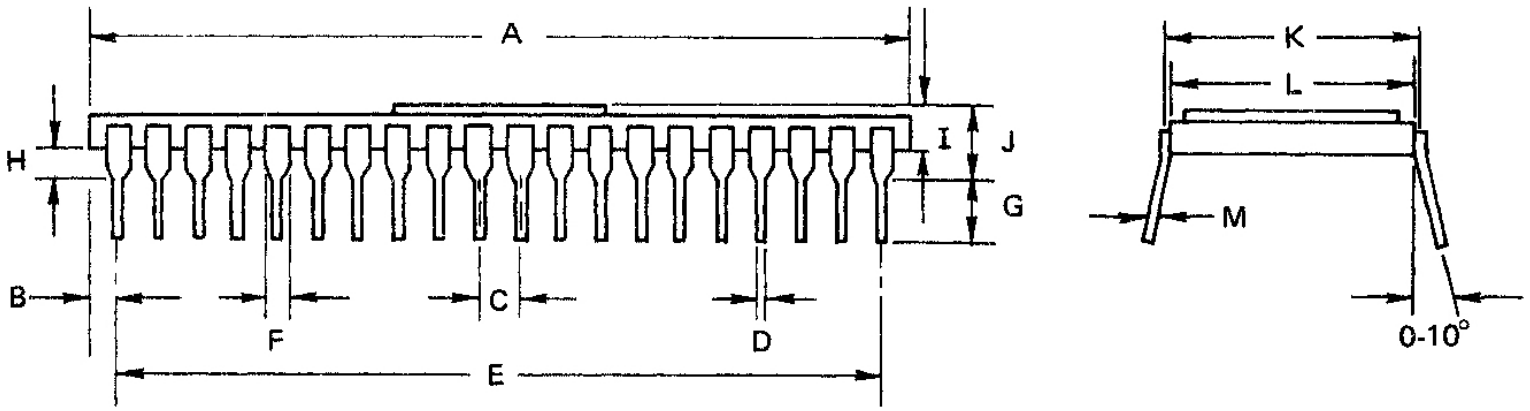


NOTE: (1) The coprocessor may not drive the buses outside the region shown without risking contention.

*for Maximum Mode only



*for Minimum Mode only



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ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.03 MAX.
B	1.62 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.0019