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μPD7210 INTELLIGENT GPIB CONTROLLER

Description

The μPD7210 is an intelligent, general purpose interface bus (GPIB) controller designed to meet all of the functional requirements for talker, listener, and controller (TLC) as specified by IEEE Standard 488-1978. Connected between a processor bus and the GPIB, the controller provides high-level management of the GPIB to unburden the processor and to simplify both hardware and software design. The μPD7210 is fully compatible with most processor architectures and requires only the addition of bus driver/receiver components to implement any type of GPIB.

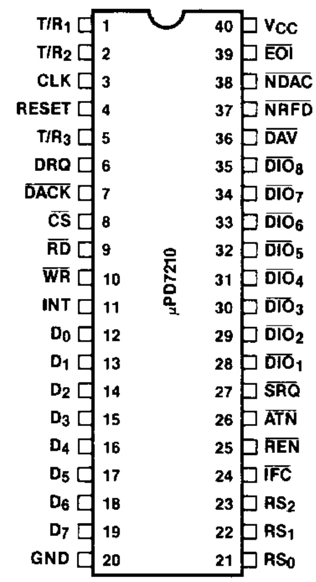
Features

- All-functional interface capability meeting IEEE Standard 488-1978
  - —SH1 (source handshake)
  - —AH1 (acceptor handshake)
  - —L3 or LE3 (listener or extended listener)
  - —T5 or TE5 (talker or extended talker)
  - —SR1 (service request)
  - —RL1 (remote local)
  - —PP1 or PP2 (parallel poll, remote or local configuration)
  - —DC1 (device clear)
  - —DT1 (device trigger)
  - —C1-C5 (controller, all functions)
- Programmable data transfer rate
- 16 MPU accessible registers: 8 read and 8 write
- 2 address registers
  - —Detection of MTA, MLA, MSA (my talk/my listen/my secondary addresses)
  - —2 device addresses
- EOS message automatic detection
- Command (IEEE Standard 488-1978) automatic processing and undefined command read capability
- DMA capability
- Programmable bus transceiver I/O specification (works with T.I./Motorola/Intel)
- 1-MHz to 8-MHz clock range
- TTL-compatible
- NMOS
- +5 V single power supply
- 8080/85/86-compatible

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7210C	40-pin plastic DIP	8 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1, 2, 5	T/R_1-T/R_3	Transmit/receive control outputs
3	CLK	Clock input
4	RESET	Reset input
6	DRQ	DMA request output
7	$\overline{DACK}$	DMA acknowledge input
8	$\overline{CS}$	Chip select input
9	$\overline{RD}$	Read input
10	$\overline{WR}$	Write input
11	INT	Interrupt request output
12-19	D_0-D_7	Bidirectional data bus
20	GND	Ground
21-23	RS_0-RS_2	Register select input
24	$\overline{IFC}$	Interface clear I/O
25	$\overline{REN}$	Remote enable I/O
26	$\overline{ATN}$	Attention control line I/O
27	$\overline{SRQ}$	Service request I/O
28-35	$\overline{DIO_1}$-$\overline{DIO_8}$	8-bit bidirectional data bus
36	$\overline{DAV}$	Data valid I/O
37	$\overline{NRFD}$	Ready for data I/O
38	$\overline{NDAC}$	Data accepted I/O
39	$\overline{EOI}$	End or identify I/O
40	V_{CC}	+5 V power supply

Pin Functions

T/R_1-T/R_3 [Transmit/Receive Control]

This is the input/output control signal for the GPIB transceivers. The values of TRM1 and TRM0 of the address mode register determine the functions of T/R_2 and T/R_3.

CLK [Clock]

This 1-MHz to 8-MHz reference clock generates the state change prohibit times T_1, T_6, T_7, and T_9 specified in IEEE Standard 488-1978.

RESET

When high, the RESET signal places the μPD7210 in an idle state.

DRQ [DMA Request]

DRQ becomes low on input of the DMA acknowledge signal $\overline{\text{DACK}}$.

$\overline{\text{DACK}}$ [DMA Acknowledge]

This signal connects the computer system data bus to the data register of the μPD7210.

$\overline{\text{CS}}$ [Chip Select]

The chip select input enables access to the register selected by the read or write operation (RS_0-RS_2).

$\overline{\text{RD}}$ [Read]

The read input places the contents of the read register specified by RS_0-RS_2 on the computer bus (D_0-D_7).

$\overline{\text{WR}}$ [Write]

This input writes data on D_0-D_7 into the write register specified by RS_0-RS_2.

INT, $\overline{\text{INT}}$ [Interrupt Request]

This output is active high/low. It becomes active due to any one of 13 internal interrupt factors (unmasked). Its active state is software configurable, and it is active high on chip reset.

D_0-D_7 [Data Bus]

The 8-bit bidirectional data bus interfaces to the computer system.

GND [Ground]

This is the ground.

RS_0-RS_2 [Register Select]

These lines select one of eight read (write) registers during a read (write) operation.

$\overline{\text{IFC}}$ [Interface Clear]

This bidirectional control line is used for clearing the interface functions.

$\overline{\text{REN}}$ [Remote Enable]

This bidirectional control line is used to select remote or local control of the devices.

$\overline{\text{ATN}}$ [Attention]

This bidirectional control line indicates whether data on the $\overline{\text{DIO}}$ lines is an interface message or a device-dependent message.

$\overline{\text{SRQ}}$ [Service Request]

This bidirectional control line is used to request service from the controller.

$\overline{\text{DIO}}_1$-$\overline{\text{DIO}}_8$ [Data Input/Output]

This 8-bit bidirectional bus transfers messages on the GPIB.

$\overline{\text{DAV}}$ [Data Valid]

This handshake line indicates that data on the $\overline{\text{DIO}}$ line is valid.

$\overline{\text{NRFD}}$ [Ready for Data]

This handshake line indicates that the device is ready for data.

$\overline{\text{NDAC}}$ [Data Accepted]

This handshake line indicates the completion of message reception.

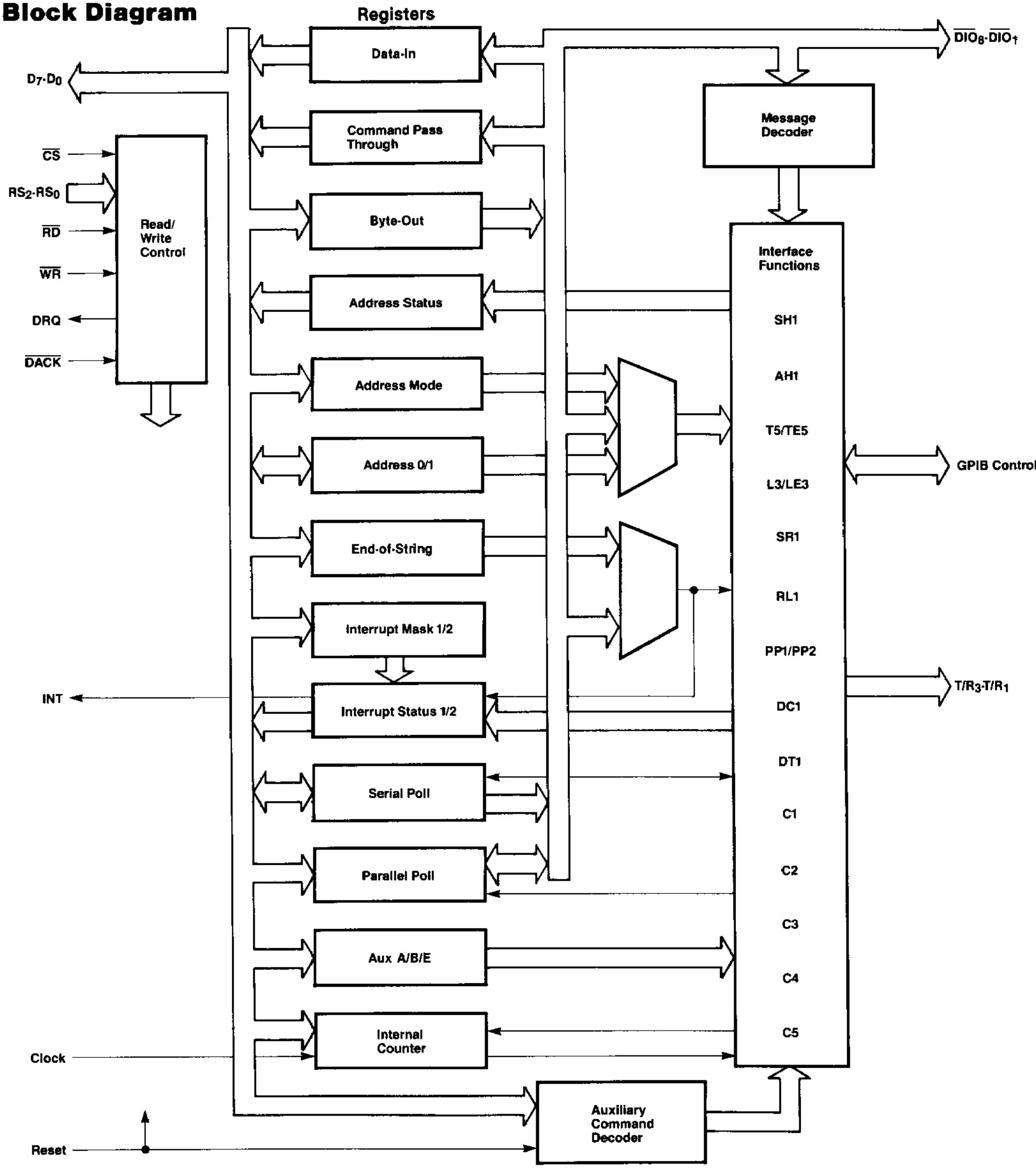
$\overline{\text{EOI}}$ [End or Identify]

This control line is used to indicate the end of a multiple byte transfer sequence or to execute parallel polling in conjunction with $\overline{\text{ATN}}$.

V_{CC} [Power Supply]

+5 V power supply.

Block Diagram



Absolute Maximum Ratings

$T_A = +25°C$

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to +7.0 V
Output voltage, V_O	−0.5 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL}	−0.5		+0.8	V	
Input high voltage	V_{IH}	+2.0		V_{CC} +0.5	V	
Low-level output voltage	V_{OL}			+0.45	V	$I_{OL} = 2$ mA (4 mA: T/R_1 pin)
High-level output voltage (except INT)	V_{OH1}	+2.4			V	$I_{OH} = -400\ \mu A$
High-level output voltage (INT)	V_{OH2}	+2.4			V	$I_{OH} = -400\ \mu A$
		+3.5				$I_{OH} = -50\ \mu A$
Input leakage current	I_{IL}	−10		+10	μA	$V_I = 0$ V to V_{CC}
Output leakage current	I_{OL}	−10		+10	μA	$V_O = 0.45$ V to V_{CC}
Supply current	I_{CC}			+180	mA	

Capacitance

$T_A = +25°C$; $V_{CC} = GND = 0\ V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			10	pF	f = 1 MHz
Output capacitance	C_{OUT}			15	pF	All pins except pin under test tied to ac ground.
I/O capacitance	$C_{I/O}$			20	pF	

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5\ V \pm 10\%$

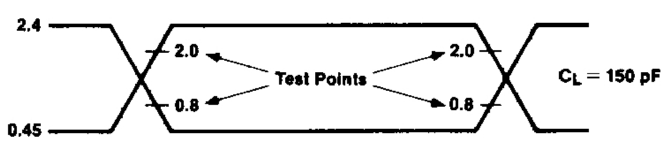
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{EOI}\downarrow \rightarrow \overline{DIO}$	t_{EODI}			250	ns	PPSS → PPAS, ATN = true
$\overline{EOI}\downarrow \rightarrow T/R_1\uparrow$	t_{EOT11}			155	ns	PPSS → PPAS, ATN = true
$\overline{EOI}\uparrow \rightarrow T/R_1\downarrow$	t_{EOT12}			200	ns	PPAS → PPSS, ATN = false
$\overline{ATN}\downarrow \rightarrow \overline{NDAC}\downarrow$	t_{ATND}			155	ns	AIDS → ANRS, LIDS
$\overline{ATN}\downarrow \rightarrow T/R_1\downarrow$	t_{ATT1}			155	ns	TACS + SPAS → TADS, CIDS
$\overline{ATN}\downarrow \rightarrow T/R_2\downarrow$	t_{ATT2}			200	ns	TACS + SPAS → TADS, CIDS
$\overline{DAV}\downarrow \rightarrow DRQ$	t_{DVRQ}			600	ns	ACRS → ACDS, LACS
$\overline{DAV}\downarrow \rightarrow \overline{NRFD}\downarrow$	t_{DVNR1}			350	ns	ACRS → ACDS
$\overline{DAV}\downarrow \rightarrow \overline{NDAC}\uparrow$	t_{DVND1}			650	ns	ACRS → ACDS → AWNS
$\overline{DAV}\uparrow \rightarrow \overline{NDAC}\downarrow$	t_{DVND2}			350	ns	AWNS → ANRS
$\overline{DAV}\uparrow \rightarrow \overline{NRFD}\uparrow$	t_{DVNR2}			350	ns	AWNS → ANRS → ACRS
$\overline{RD}\downarrow \rightarrow \overline{NRFD}\uparrow$	t_{RNR}			500	ns	ANRS → ACRS LACS, DI register selected
$\overline{NDAC}\uparrow \rightarrow DRQ\uparrow$	t_{NDRQ}			400	ns	STRS → SWNS → SGNS, TACS
$\overline{NDAC}\uparrow \rightarrow \overline{DAV}\uparrow$	t_{NDDV}			350	ns	STRS → SWNS → SGNS
$\overline{WR}\uparrow \rightarrow \overline{DIO}$	t_{WDI}			250	ns	SGNS → SDYS, BO register selected
$\overline{NRFD}\uparrow \rightarrow \overline{DAV}\downarrow$	t_{NRDV}			350	ns	SDYS → STRS, T_1 = true
$\overline{WR}\uparrow \rightarrow \overline{DAV}\downarrow$	t_{WDV}			830 + t_{SYNC}	ns	SGNS → SDYS → STRS; BO register selected; RFD = true; N_F = fc = 8 MHz; T_1 (high speed)
TRIG pulse width	t_{TRIG}	50			ns	

AC Characteristics (cont)

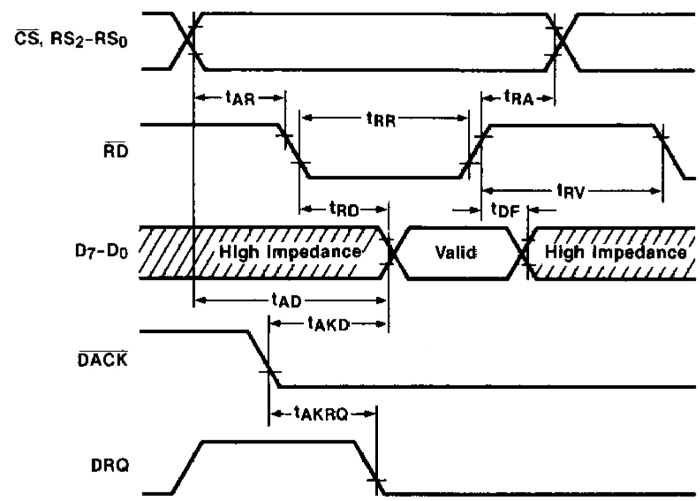
Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Address setup to $\overline{RD}$	t_{AR}	85			ns	RS_0 to RS_2
		0			ns	$\overline{CS}$
Address hold from $\overline{RD}$	t_{RA}	0			ns	
$\overline{RD}$ pulse width	t_{RR}	170			ns	
Data delay from address	t_{AD}			250	ns	
Data delay from $\overline{RD}$↓	t_{RD}			150	ns	
Output float delay from $\overline{RD}$↑	t_{DF}	0		80	ns	
$\overline{RD}$ recovery time	t_{RV}	250			ns	
Address setup to $\overline{WR}$	t_{AW}	0			ns	
Address hold from $\overline{WR}$	t_{WA}	0			ns	
$\overline{WR}$ pulse width	t_{WW}	170			ns	
Data setup to $\overline{WR}$	t_{DW}	150			ns	
Data hold from $\overline{WR}$	t_{WD}	0			ns	
$\overline{WR}$ recovery time	t_{RV}	250			ns	
DRQ↓ delay from selected $\overline{DACK}$	t_{AKRQ}			130	ns	
Data delay from $\overline{DACK}$	t_{AKD}			200	ns	
$\overline{DACK}$ hold time from $\overline{WR}$↑	t_{DH}	200			ns	

Timing Waveforms

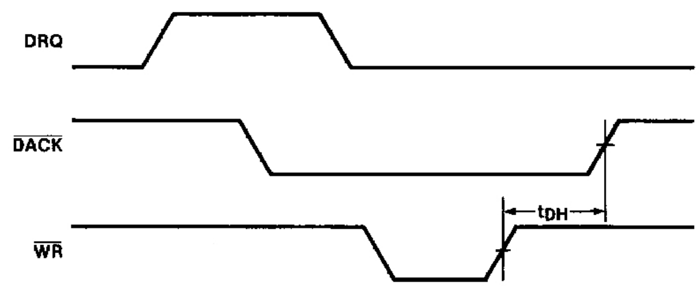
Test Waveform



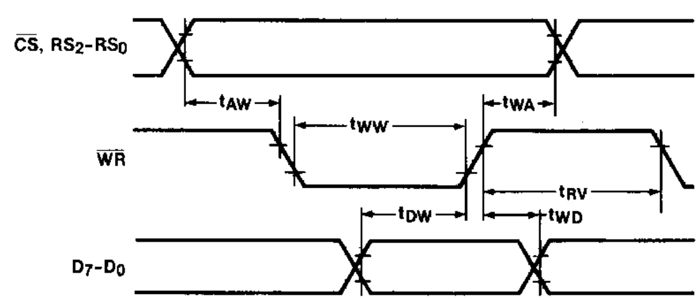
DMA Read



DMA Write



CPU Write



History

The IEEE Standard 488 describes a "Standard Digital Interface for Programmable Instrumentation" which, since its introduction in 1975, has become the most popular means of interconnecting instruments and controllers in laboratory, automatic test, and even industrial applications. Refined over several years, the 488-1978 Standard, also known as the General Purpose Interface Bus (GPIB), is a highly sophisticated standard providing a high degree of flexibility to meet virtually all instrumentation requirements. The μPD7210 implements all of the functions that are required to interface to the GPIB. While it is beyond the scope of this document to provide a complete explanation of the IEEE 488 Standard, a basic description follows:

The GPIB interconnects up to 15 devices over a common set of data control lines. Three types of devices are defined by the standard: talker, listener, and controller, although some devices may combine functions such as talker/listener or talker/controller.

Data on the GPIB is transferred in a bit-parallel, byte-serial fashion over eight data I/O lines ($\overline{DIO}_1$-$\overline{DIO}_8$). A three-wire handshake is used to ensure synchronization of transmission and reception. In order to permit more than one device to receive data at the same time, these control lines are "open collector" so that the slowest device controls the data rate. A number of other control lines perform a variety of functions such as device addressing, interrupt generation, and so forth.

The μPD7210 implements all functional aspects of talker, listener, and controller functions as defined by the 488-1978 Standard on a single chip.

General

The μPD7210 is an intelligent controller designed to provide high-level protocol management of the GPIB, freeing the host processor for other tasks. Control of the μPD7210 is accomplished via 16 internal registers. Data may be transferred either under program control or via DMA using the μPD7210's DMA control facilities to further reduce processor overhead. The processor interface of the μPD7210 is general in nature and may be readily interfaced to most processor lines.

In addition to providing all control and data lines necessary for a complete GPIB implementation, the μPD7210 also provides a unique set of bus transceiver controls permitting a variety of transceiver configurations for maximum flexibility.

Internal Registers

The μPD7210 has eight read registers (0R-7R) and eight write registers (0W-7W). The register number is selected via the RS_2, RS_1, and RS_0 lines; read or write is selected via WR, RD, and CS.

Register Addressing

		Addressing					
Register		**RS_2**	**RS_1**	**RS_0**	**WR**	**RD**	**CS**
Data-In	0R	0	0	0	1	0	0
Interrupt Status 1	1R	0	0	1	1	0	0
Interrupt Status 2	2R	0	1	0	1	0	0
Serial Poll Status	3R	0	1	1	1	0	0
Address Status	4R	1	0	0	1	0	0
Command Pass Through	5R	1	0	1	1	0	0
Address 0	6R	1	1	0	1	0	0
Address 1	7R	1	1	1	1	0	0
Byte Out	0W	0	0	0	0	1	0
Interrupt Mask 1	1W	0	0	1	0	1	0
Interrupt Mask 2	2W	0	1	0	0	1	0
Serial Poll Mode	3W	0	1	1	0	1	0
Address Mode	4W	1	0	0	0	1	0
Auxiliary Mode	5W	1	0	1	0	1	0
Address 0/1	6W	1	1	0	0	1	0
End of String	7W	1	1	1	0	1	0

Data Registers

Data-In (0R)

DI_7	DI_6	DI_5	DI_4	DI_3	DI_2	DI_1	DI_0

Byte-Out (0W)

BO_7	BO_6	BO_5	BO_4	BO_3	BO_2	BO_1	BO_0

The data registers are used for data and command transfers between the GPIB and the microcomputer system. The Data-In register holds data sent from the GPIB to the computer; the Byte-Out register holds information written into it for transfer to the GPIB.

Interrupt Registers

Interrupt Status 1 (1R)

CPT	APT	DET	END	DEC	ERR	DO	DI

Interrupt Status 2 (2R)

INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC

Interrupt Mask 1 (1W)

CPT	APT	DET	END	DEC	ERR	DO	DI

Interrupt Mask 2 (2W)

0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC

The interrupt registers are composed of interrupt status bits, interrupt mask bits, and some other non-interrupt related bits.

There are 13 factors that can generate an interrupt from the μPD7210, each with its own status bit and mask bit.

The interrupt status bits are always set to 1 if the interrupt condition is met. The interrupt mask bits decide whether or not the INT bit and the interrupt pin will be active for that condition.

Interrupt Status Bits

INT	OR of all unmasked interrupt status bits
CPT	Command pass through
APT	Address pass through
DET	Device trigger
END	End (END or EOS message received)
DEC	Device clear
ERR	Error
DO	Data out
DI	Data in
SRQI	Service request input
LOKC	Lockout change
REMC	Remote change
ADSC	Address status change
CO	Command output

Noninterrupt Related Bits

LOK	Lockout
REM	Remote/local
DMAO	Enable/disable DMA out
DMAI	Enable/disable DMA in

Serial Poll Registers

Serial Poll Status (3R)

S_8	PEND	S_6	S_5	S_4	S_3	S_2	S_1

Serial Poll Mode (3W)

S_8	rsv	S_6	S_5	S_4	S_3	S_2	S_1

The serial poll mode register holds the STB (status byte: S_8, S_6-S_1) sent over the GPIB and the local message rsv (request service). The serial poll mode register may be read through the serial poll status register. The PEND is set by rsv = 1 and cleared by NPRS · $\overline{\text{rsv}}$ = 1 (NPRS means negative poll response state).

Address Mode/Address Status Registers

Address Status (4R)

CIC	$\overline{\text{ATN}}$	SPMS	LPAS	TPAS	LA	TA	MJMN

Address Mode (4W)

t_{on}	l_{on}	TRM1	TRM0	0	0	AMD1	AMD0

The address mode register selects the address mode of the device and also sets the mode for the transceiver control lines, T/R_3 and T/R_2.

The functions of T/R_2 (pin 2) and T/R_3 (pin 5) are determined by the TRM1, TRM0 values of the address mode register.

Function of T/R_2 and T/R_3

T/R_2	T/R_3	TRM1	TRM0
EOIOE	TRIG	0	0
CIC	TRIG	0	1
CIC	EOIOE	1	0
CIC	PE	1	1

EOIOE = TACS + SPAS + CIC · $\overline{\text{CSBS}}$
This denotes the input/output of the $\overline{\text{EOI}}$ terminal.
When 1: output
When 0: input

CIC = $\overline{\text{CIDS + CADS}}$
This denotes whether or not the controller interface function is active.
When 1: $\overline{\text{ATN}}$ = output, $\overline{\text{SRQ}}$ = input
When 0: $\overline{\text{ATN}}$ = input, $\overline{\text{SRQ}}$ = output

PE = CIC + $\overline{\text{PPAS}}$
This indicates the type of bus driver connected to the $\overline{\text{DIO}}_8$ to $\overline{\text{DIO}}_1$ and $\overline{\text{DAV}}$ lines.
When 1: three-state
When 0: open-collector

TRIG: When DTAS state is initiated or when a trigger auxiliary command is issued, a high pulse is generated.

Upon reset, TRM0 and TRM1 become 0 (TRM0 = TRM1 = 0) and a local message port is provided so that T/R_2 and T/R_3 both become low.

Address Modes

t_{on}	l_{on}	ADM1	ADM0	Address Mode	Contents of Address 0 Register	Contents of Address 1 Register
1	0	0	0	Talk only mode	Address identification not necessary (No controller on the GPIB)	
0	1	0	0	Listen only mode	Not used	
0	0	0	1	Address mode 1 (Note 1)	Major talk address or major listen address	Minor talk address or minor listen address
0	0	1	0	Address mode 2 (Note 2)	Primary address (talk or listen)	Secondary address (talk or listen)
0	0	1	1	Address mode 3 (Note 3)	Primary address (major talk or major listen)	Primary address (minor talk or minor listen)

Note:

(1) Either MTA or MLA reception is indicated by coincidence of either address with the received address, interface function T or L.

(2) Address register 0 = primary; address register 1 = secondary; interface function TE or LE.

(3) CPU must read secondary address via Command Pass Through register interface function (TE or LE).

(4) Combinations other than those indicated are prohibited.

Address Status Bits

$\overline{\text{ATN}}$	Data transfer cycle (device in CSBS)
LPAS	Listener primary addressed state
TPAS	Talker primary addressed state
CIC	Controller active
LA	Listener addressed
TA	Talker addressed
MJMN	Sets minor T/L address, reset = major T/L address
SPMS	Serial poll mode state

Address Registers

Address 0 (6R)

X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD-1

Address 1 (7R)

EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1

Address 0/1 (6W)

ARS	DT	DL	AD_5	AD_4	AD_3	AD_2	AD_1

The µPD7210 is able to detect automatically two types of addresses that are held in address registers 0 and 1. The addressing modes are outlined below.

Address settings are made by writing into the address 0/1 register. The function of each bit is described below.

Address 0/1 Register Bit Selections

ARS	Selects either address register 0 or 1
DT	Permits or prohibits address to be detected as Talk
DL	Permits or prohibits address to be detected as Listen
AD_5-AD_1	Device address value
EOI	Holds the value of EOI line when data is received

Command Pass Through Register [5R]

CPT_7	CPT_6	CPT_5	CPT_4	CPT_3	CPT_2	CPT_1	CPT_0

The CPT register is used such that the CPU may read the DIO lines in the cases of undefined command, secondary address, or parallel poll response.

End-of-String Register [7W]

EC_7	EC_6	EC_5	EC_4	EC_3	EC_2	EC_1	EC_0

This register holds either a 7- or 8-bit EOS message byte used in the GPIB system to detect the end of a data block. Auxiliary register A controls the specific use of this register.

Auxiliary Mode Register [5W]

CNT_2	CNT_1	CNT_0	COM_4	COM_3	COM_2	COM_1	COM_0

This is a multipurpose register. A write to this register generates one of the following operations according to the values of the CNT bits.

Auxiliary Mode Operations

CNT 2	1	0	COM 4	3	2	1	0	Operation
0	0	0	C_4	C_3	C_2	C_1	C_0	Issues an auxiliary command specified by C_4 to C_0.
0	0	1	0	F_3	F_2	F_1	F_0	The reference clock frequency is specified and T_1, T_6, T_7, and T_9 are determined as a result.
0	1	1	U	S	P_3	P_2	P_1	Makes a write operation to the parallel poll register.
1	0	0	A_4	A_3	A_2	A_1	A_0	Makes a write operation to the auxiliary A register.
1	0	1	B_4	B_3	B_2	B_1	B_0	Makes a write operation to the auxiliary B register.
1	1	0	0	0	0	E_1	E_0	Makes a write operation to the auxiliary E register.

Commands and Other Registers

Auxiliary Commands

0	0	0	C_4	C_3	C_2	C_1	C_0

Auxiliary Command Descriptions

Command C_4	C_3	C_2	C_1	C_0	Auxiliary Command	Description
0	0	0	0	0	iepon	Immediate execute pon; generate local pon message.
0	0	0	1	0	crst	Chip reset (same as external reset)
0	0	0	1	1	rrfd	Release RFD
0	0	1	0	0	trig	Trigger
0	0	1	0	1	rtl	Return to local message generation
0	0	1	1	0	seoi	Send EOI message
0	0	1	1	1	nvid	Nonvalid (OSA reception); release DAC holdoff
0	1	1	1	1	vid	Valid (MSA Reception, CPT, DEC, DET); release DAC holdoff
0	X	0	0	1	sppf	Set/reset parallel poll flag
1	0	0	0	0	gts	Go to standby
1	0	0	0	1	tca	Take control asynchronously

Auxiliary Command Descriptions (cont)

Command C_4	C_3	C_2	C_1	C_0	Auxiliary Command	Description
1	0	0	1	0	tcs	Take control synchronously
1	1	0	1	0	tcse	Take control synchronously on end
1	0	0	1	1	ltn	Listen
1	1	0	1	1	ltnc	Listen with continuous mode
1	1	1	0	0	lun	Local unlisten
1	1	1	0	1	epp	Execute parallel poll
1	X	1	1	0	sifc	Set/reset IFC
1	X	1	1	1	sren	Set/reset REN
1	0	1	0	0	dsc	Disable system control

Internal Counter

0	0	1	0	F_3	F_2	F_1	F_0

The internal counter generates the state change prohibit times (T_1, T_6, T_7, T_9) specified in IEEE Standard 488-1978 with reference to the clock frequency.

Auxiliary A Register

1	0	0	A_4	A_3	A_2	A_1	A_0

Of the five bits that may be specified as part of the access word, two bits control the GPIB data receiving modes of the μPD7210 and three bits control how the end-of-string (EOS) message is used.

Data Receiving Modes

A_1	A_0	Data Receiving Mode
0	0	Normal handshake mode
0	1	RFD holdoff on all data modes
1	0	RFD holdoff on end mode
1	1	Continuous mode

EOS Message

Bit Name			Function
A_2	0	Prohibit	Permits (prohibits) the setting of the END bit by reception of the EOS message.
	1	Permit	
A_3	0	Prohibit	Permits (prohibits) automatic transmission of END message simultaneously with the transmission of EOS message TACS.
	1	Permit	
A_4	0	7-bit EOS	Makes the 8 bits (7 bits) of the EOS register the valid EOS message.
	1	8-bit EOS	

Auxiliary B Register

1	0	1	B_4	B_3	B_2	B_1	B_0

The auxiliary B register is much like the A register in that it controls the special operating features of the device.

Special Features

Bit Name			Function
B_0	1	Permit	Permits (prohibits) the detection of an undefined command. In other words, it permits (prohibits) the setting of the CPT bit on receipt of an undefined command.
	0	Prohibit	
B_1	1	Permit	Permits (prohibits) the transmission of the END message when in serial poll active state (SPAS).
	0	Prohibit	
B_2	1	T_1 (high-speed)	T_1 (high speed) as T_1 in source handshake function after transmission of second byte following data transmission.
	0	T_1 (low-speed)	Sets T_1 (low speed) as T_1 in all cases.
B_3	1	$\overline{\text{INT}}$	Specifies the active level of the $\overline{\text{INT}}$ pin.
	0	INT	
B_4	1	ist = SRQS	SRQS indicates the value of the ist level local message (the value of the parallel poll flag is ignored). SRQS = 1 . . . ist = 1 SRQS = 0 . . . ist = 0
	0	ist = Parallel Poll Flag	The value of the parallel poll flag is taken as the ist local message.

Auxiliary E Register

1	1	0	0	0	0	E_1	E_0

This register controls the Data Acceptance modes of the μPD7210.

Data Acceptance Modes

Bit Name			Function
E_0	1	Enable	DAC holdoff by initialization of DCAS
	0	Disable	
E_1	1	Enable	DAC holdoff by initialization of DTAS
	0	Disable	

Parallel Poll Register

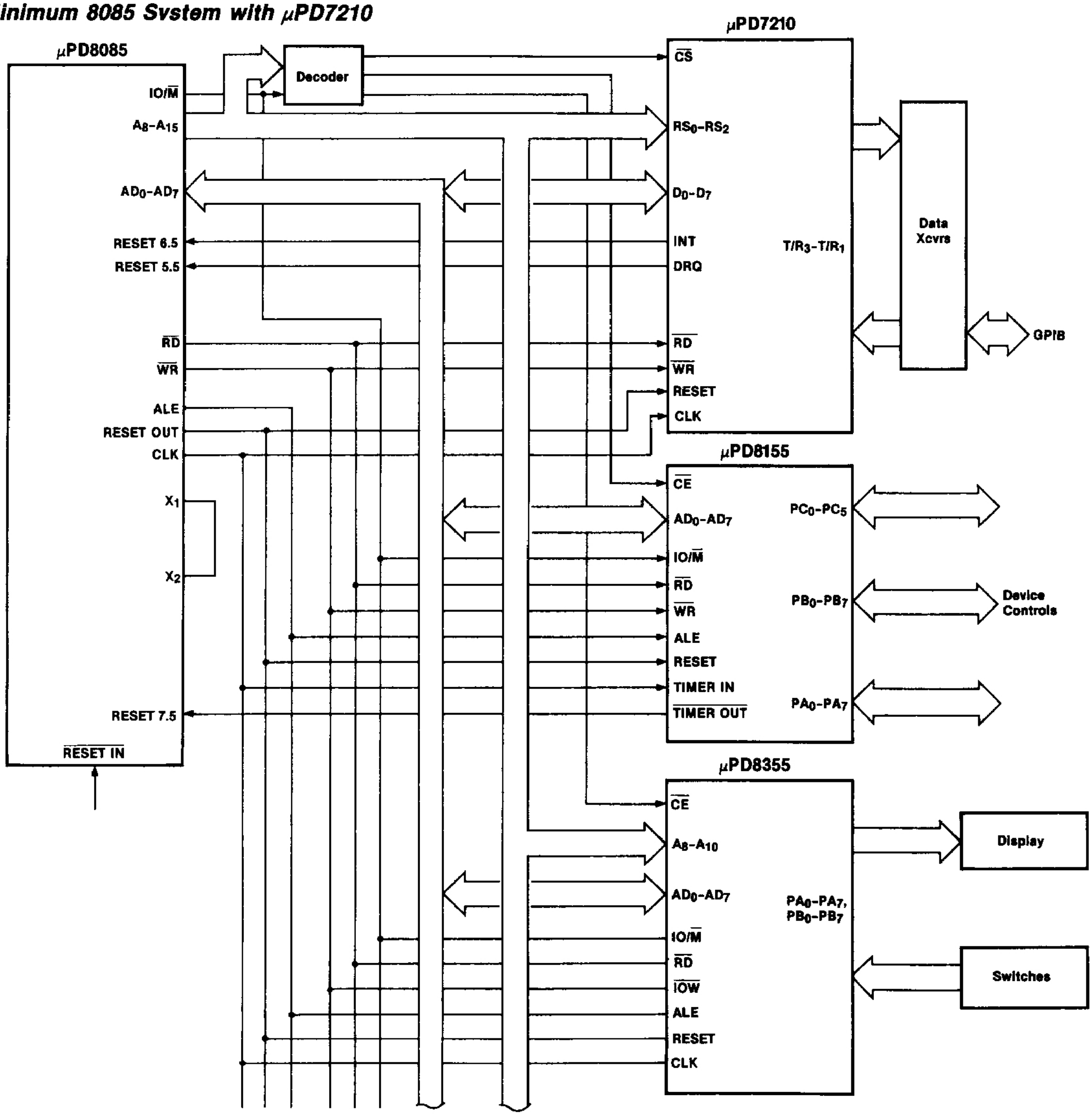
0	1	1	U	S	P_3	P_2	P_1

The parallel poll register defines the parallel poll response of the μPD7210.

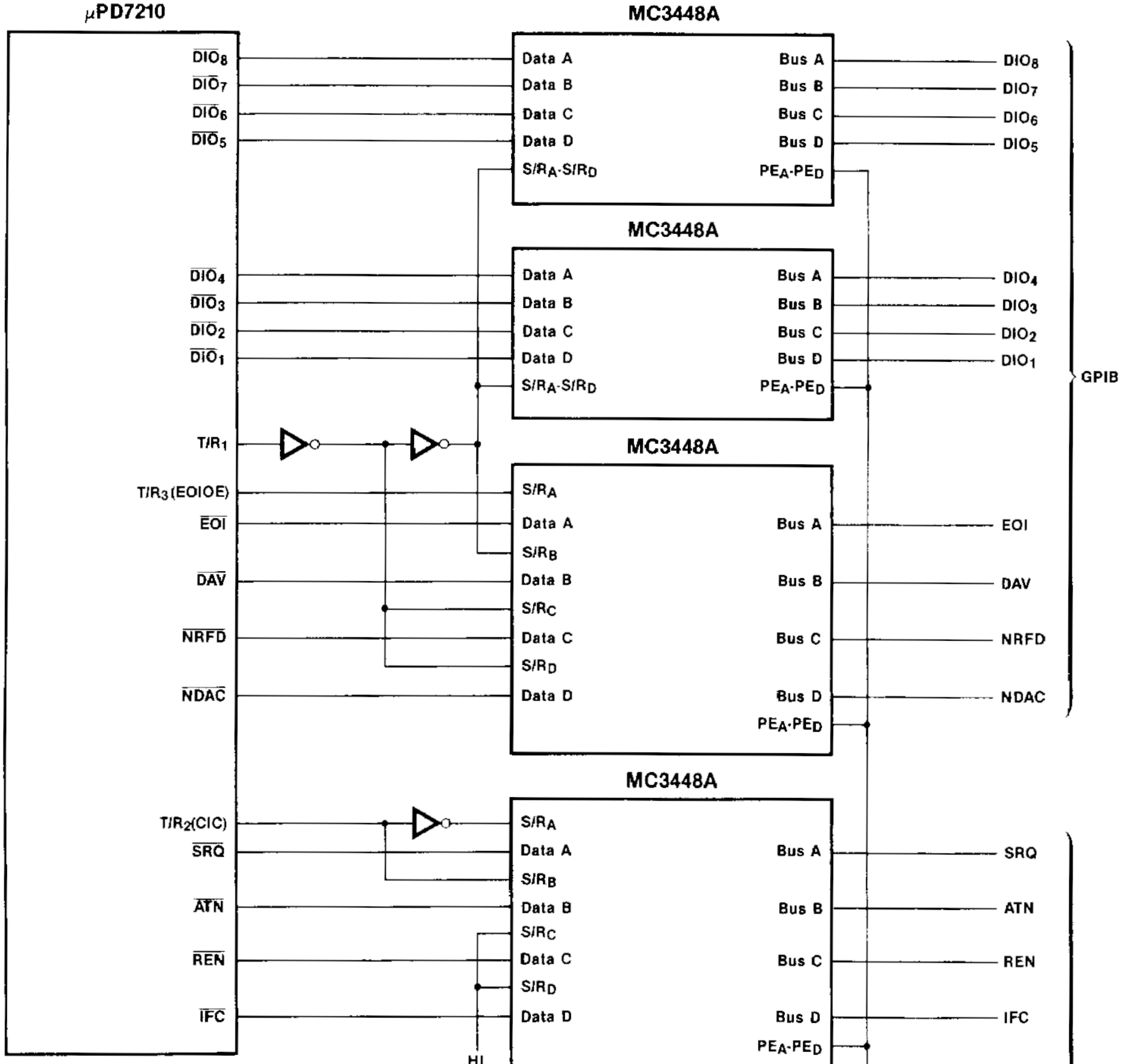
Parallel Poll Response

Bit Name		Function
U	1	No response to parallel poll
	0	Response to parallel poll
S	1	In phase
	0	Reverse phase
P_3-P_1	000-111	Status bit output line DIO_1 to DIO_8

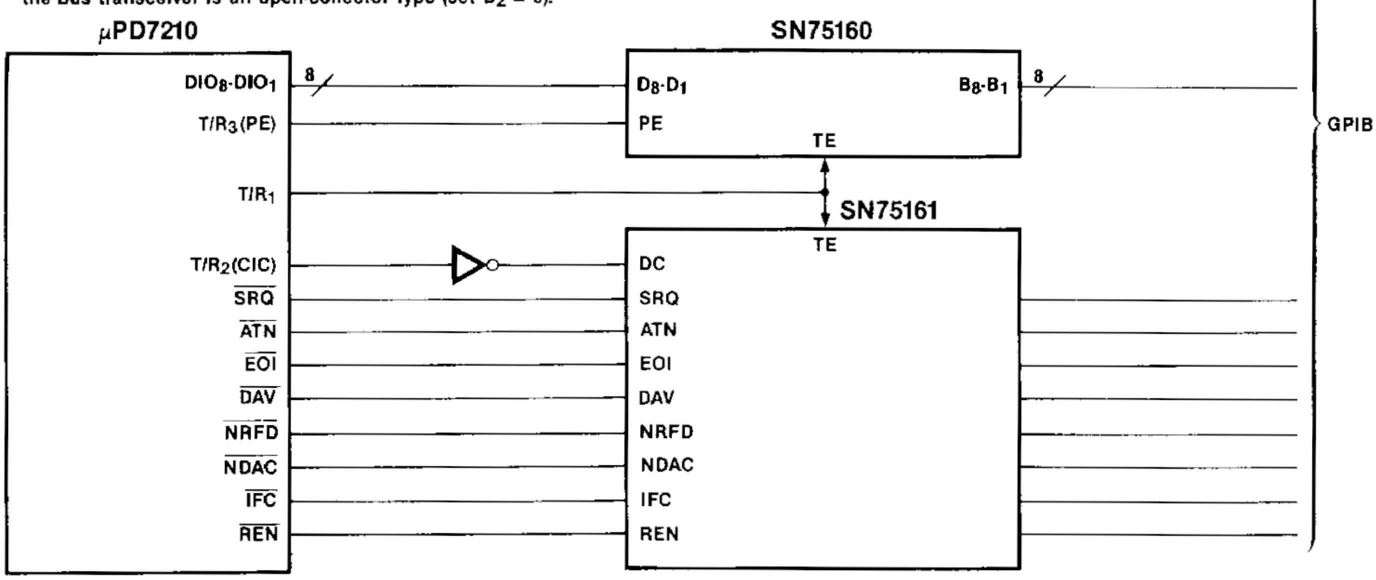
Minimum 8085 System with μPD7210



Minimum 8085 System with μPD7210 (cont)



Note: In this example, high speed data transfer cannot be made since the bus transceiver is an open-collector type (set $B_2 = 0$).



Note: In the case of low-speed data transfer ($B_2 = 0$), the T/R_3 pin can be used as a TRIG output. The PE input of SN75160 should be cleared to 0.