# 65,536 x 1 BIT DYNAMIC RANDOM ACCESS MEMORY

**DESCRIPTION**

The NEC $\mu$PD4164 is a 65,536 words by 1 bit Dynamic N-Channel MOS RAM designed to operate from a single +5V power supply. The negative-voltage substrate bias is internally generated — its operation is both automatic and transparent.

The $\mu$PD4164 utilizes a double-poly-layer N-channel silicon gate process which provides high storage cell density, high performance and high reliability.

The $\mu$PD4164 uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, including the 512 sense amplifiers, which assures that power dissipation is minimized. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between Dynamic RAM generations.

The $\mu$PD4164 three-state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state. The $\mu$PD4164 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$ only refresh cycles.
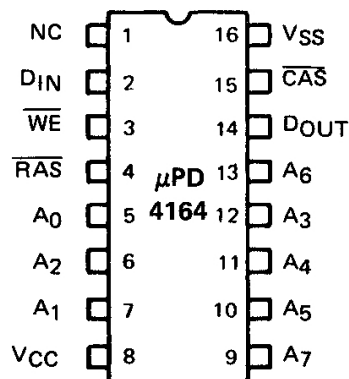
Refreshing is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of $A_0$ through $A_6$ during a 2 ms period.

Multiplexed address inputs permit the $\mu$PD4164 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

**FEATURES**

- High Memory Density
- Multiplexed Address Inputs
- Single +5V Supply
- On Chip Substrate Bias Generator
- Access Time: $\mu$PD4164-1 — 250 ns
  $\mu$PD4164-2 — 200 ns
  $\mu$PD4164-3 — 150 ns
- Read, Write Cycle Time: $\mu$PD4164-1 — 410 ns
  $\mu$PD4164-2 — 335 ns
  $\mu$PD4164-3 — 270 ns
- Low Power Dissipation: 250 mW (Active); 28 mW (Standby)
- Non-Latched Output is Three-State, TTL Compatible
- Read, Write, Read-Write; Read-Modify-Write, RAS Only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Input Capacitance
- 128 Refresh Cycles ($A_0$-$A_6$ Pins for Refresh Address)
- CAS Controlled Output Allows Hidden Refresh
- Available in Both Ceramic and Plastic 16 Pin Packages

**PIN CONFIGURATION**

| | | |
|---|---|---|
| NC | 1 | 16 V_SS |
| D_IN | 2 | 15 $\overline{CAS}$ |
| $\overline{WE}$ | 3 | 14 D_OUT |
| $\overline{RAS}$ | 4 | 13 A_6 |
| A_0 | 5 | 12 A_3 |
| A_2 | 6 | 11 A_4 |
| A_1 | 7 | 10 A_5 |
| V_CC | 8 | 9 A_7 |

$\mu$PD 4164

**PIN NAMES**

| | |
|---|---|
| $A_0$-$A_7$ | Address Inputs |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{WE}$ | Write Enable |
| $D_{IN}$ | Data Input |
| $D_{OUT}$ | Data Output |
| $V_{CC}$ | Power Supply (+5V) |
| $V_{SS}$ | Ground |
| NC | No Connection |

Operating Temperature . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0°C to +70°C

Storage Temperature (Ceramic Package) . . . . . . . . . . . . . . . . . . . . . −55°C to +150°C

(Plastic Package) . . . . . . . . . . . . . . . . . . . . . −55°C to +125°C

Supply Voltages On Any Pin Except $V_{CC}$ . . . . . . . . . . . . . . . . . . . −1 to +7 Volts ①

Supply Voltage $V_{CC}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −0.5 to +7 Volts ①

Short Circuit Output Current . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 50 mA

Power Dissipation . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1 Watt

Note: ① Relative to $V_{SS}$

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

\*$T_a$ = 25°C

$T_a$ = 0° to 70°C  ① ; $V_{CC}$ = +5V ± 10%; $V_{SS}$ = 0V

| PARAMETER | SYMBOL | | LIMITS | | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | |
| Supply Voltage | $V_{CC}$ | | 4.5 | 5.0 | 5.5 | V | All Voltages Referenced to $V_{SS}$ |
| | $V_{SS}$ | | 0 | 0 | 0 | V | |
| High Level Input Voltage, ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$) | $V_{IHC}$ | | 2.4 | | 5.5 | V | |
| High Level Input Voltage, All Inputs Except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | $V_{IH}$ | | 2.4 | | 5.5 | V | |
| Low Level Input Voltage, All Inputs | $V_{IL}$ | | -2.0 | | 0.8 | V | |
| Operating Current Average Power Supply Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling; $t_{RC}$ = $t_{RC}$ (Min.) | $I_{CC1}$ | μPD4164-1 | | | 45 | mA | ② |
| | | μPD4164-2 | | | 50 | | |
| | | μPD4164-3 | | | 60 | | |
| Standby Current Power Supply Standby Current ($\overline{RAS}$ = $V_{IHC}$, $D_{OUT}$ = Hi-Impedance) | $I_{CC2}$ | | | | 5.0 | mA | |
| Refresh Current Average Power Supply Current, Refresh Mode; $\overline{RAS}$ Cycling, $\overline{CAS}$ = $V_{IHC}$, $t_{RC}$ = $t_{RC}$ (Min.) | $I_{CC3}$ | μPD4164-1 | | | 35 | mA | ② |
| | | μPD4164-2 | | | 40 | | |
| | | μPD4164-3 | | | 45 | | |
| Page Mode Current Average Power Supply Current, Page Mode Operation $\overline{RAS}$ = $V_{IL}$; $\overline{CAS}$ Cycling $t_{PC}$ = $t_{PC}$ (Min.) | $I_{CC4}$ | μPD4164-1 | | | 35 | mA | ② |
| | | μPD4164-2 | | | 40 | | |
| | | μPD4164-3 | | | 45 | | |
| Input Leakage Current Any Input $V_{IN}$ = 0 to +5.5 Volts, All Other Pins Not Under Test = 0V | $I_{I(L)}$ | | −10 | | 10 | μA | |
| Output Leakage Current $D_{OUT}$ is Disabled, $V_{OUT}$ = 0 to +5.5 Volts | $I_{O(L)}$ | | −10 | | 10 | μA | |
| Output Levels High Level Output Voltage ($I_{OUT}$ = 5 mA) | $V_{OH}$ | | 2.4 | | $V_{CC}$ | V | |
| Low Level Output Voltage ($I_{OUT}$ = 4.2 mA) | $V_{OL}$ | | 0 | | 0.4 | V | |

Notes: ① $T_a$ is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met.

② $I_{CC1}$, $I_{CC3}$ and $I_{CC4}$ depend on output loading and cycle rates. Specified rates are obtained with the output open.

| PARAMETER | SYMBOL | LIMITS | | | | | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | μPD4164-1 | | μPD4164-2 | | μPD4164-3 | | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Random Read or Write Cycle Time | $t_{RC}$ | 410 | | 335 | | 270 | | ns | ⑤ |
| Read Write Cycle Time | $t_{RWC}$ | 465 | | 335 | | 270 | | ns | ⑤ |
| Page Mode Cycle Time | $t_{PC}$ | 275 | | 225 | | 170 | | ns | |
| Access Time from $\overline{RAS}$ | $t_{RAC}$ | | 250 | | 200 | | 150 | ns | ⑥ ⑧ |
| Access Time from $\overline{CAS}$ | $t_{CAC}$ | | 165 | | 135 | | 100 | ns | ⑦ ⑧ |
| Output Buffer Turn-Off Delay | $t_{OFF}$ | 0 | 60 | 0 | 50 | 0 | 40 | ns | ⑨ |
| Transition Time (Rise and Fall) | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns | ④ |
| $\overline{RAS}$ Precharge Time | $t_{RP}$ | 150 | | 120 | | 100 | | ns | |
| $\overline{RAS}$ Pulse Width | $t_{RAS}$ | 250 | 10,000 | 200 | 10,000 | 150 | 10,000 | ns | |
| $\overline{RAS}$ Hold Time | $t_{RSH}$ | 165 | | 135 | | 100 | | ns | |
| $\overline{CAS}$ Pulse Width | $t_{CAS}$ | 165 | 10,000 | 135 | 10,000 | 100 | 10,000 | ns | |
| $\overline{CAS}$ Hold Time | $t_{CSH}$ | 250 | | 200 | | 150 | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Time | $t_{RCD}$ | 35 | 85 | 30 | 65 | 25 | 50 | ns | ⑩ |
| $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | $t_{CRP}$ | 0 | | 0 | | 0 | | ns | |
| $\overline{CAS}$ Precharge Time | $t_{CPN}$ | 35 | | 30 | | 25 | | ns | |
| $\overline{CAS}$ Precharge Time (For Page Mode Cycle Only) | $t_{CP}$ | 100 | | 80 | | 60 | | ns | |
| $\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time | $t_{RPC}$ | 0 | | 0 | | 0 | | ns | |
| Row Address Set-Up Time | $t_{ASR}$ | 0 | | 0 | | 0 | | ns | |
| Row Address Hold Time | $t_{RAH}$ | 25 | | 20 | | 15 | | ns | |
| Column Address Set-Up Time | $t_{ASC}$ | 0 | | 0 | | 0 | | ns | |
| Column Address Hold Time | $t_{CAH}$ | 75 | | 55 | | 45 | | ns | |
| Column Address Hold Time Referenced to $\overline{RAS}$ | $t_{AR}$ | 160 | | 120 | | 95 | | ns | |
| Read Command Set-Up Time | $t_{RCS}$ | 0 | | 0 | | 0 | | ns | |
| Read Command Hold Time Referenced to $\overline{RAS}$ | $t_{RRH}$ | 30 | | 25 | | 20 | | ns | ⑬ |
| Read Command Hold Time | $t_{RCH}$ | 0 | | 0 | | 0 | | ns | ⑬ |
| Write Command Hold Time | $t_{WCH}$ | 75 | | 55 | | 45 | | ns | |
| Write Command Hold Time Referenced to $\overline{RAS}$ | $t_{WCR}$ | 160 | | 120 | | 95 | | ns | |
| Write Command Pulse Width | $t_{WP}$ | 75 | | 55 | | 45 | | ns | |
| Write Command to $\overline{RAS}$ Lead Time | $t_{RWL}$ | 100 | | 55 | | 45 | | ns | |
| Write Command to $\overline{CAS}$ Lead Time | $t_{CWL}$ | 100 | | 55 | | 45 | | ns | |
| Data-In Set-Up Time | $t_{DS}$ | 0 | | 0 | | 0 | | ns | ⑪ |
| Data-In Hold Time | $t_{DH}$ | 75 | | 55 | | 45 | | ns | ⑪ |
| Data-In Hold Time Referenced to $\overline{RAS}$ | $t_{DHR}$ | 160 | | 120 | | 95 | | ns | |
| Refresh Period | $t_{REF}$ | | 2 | | 2 | | 2 | ms | |
| $\overline{WRITE}$ Command Set-Up Time | $t_{WCS}$ | −20 | | −20 | | −20 | | ns | ⑫ |
| $\overline{CAS}$ to $\overline{WRITE}$ Delay | $t_{CWD}$ | 115 | | 80 | | 60 | | ns | ⑫ |
| $\overline{RAS}$ to $\overline{WRITE}$ Delay | $t_{RWD}$ | 200 | | 145 | | 110 | | ns | ⑫ |

Notes:
① $T_a$ is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.

② An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

③ AC measurements assume $t_T = 5$ ns.

④ $V_{IHC}$ (min) or $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IHC}$ or $V_{IH}$ and $V_{IL}$.

⑤ The specifications for $t_{RC}$ (min) and $t_{RWC}$ (min) are used only to indicate cycle times at which proper operation over the full temperature range ($0°C \leq T_a \leq 70°C$) is assured.

⑥ Assumes that $t_{RCS} \leq t_{RCD}$ (max). If $t_{RCS}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will increase by the amount that $t_{RCD}$ exceeds the values shown.

⑦ Assumes that $t_{RCD} \geq t_{RCD}$ (max).

⑧ Measured with a load equivalent to 2 TTL loads and 100 pF.

⑨ $t_{OFF}$ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

⑩ Operation within the $t_{RCD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RCD}$ (max) is specified as a reference point only, if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.

⑪ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

⑫ $t_{WCS}$, $t_{CWD}$ and $t_{RWD}$ are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to $V_{IH}$) is indeterminate.

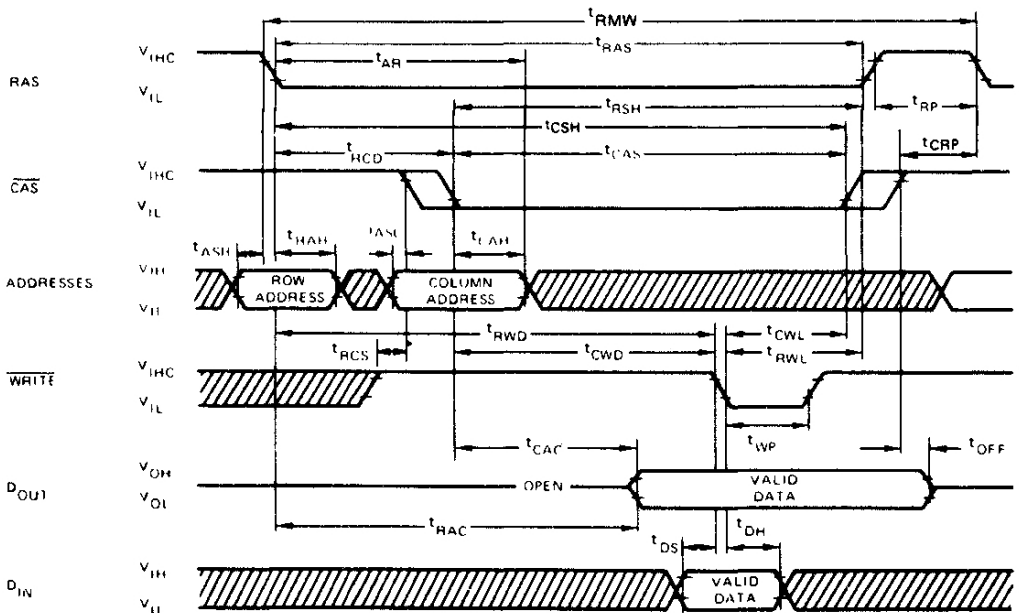⑬ Either $t_{RRH}$ or $t_{RCH}$ must be satisfied for a read cycle.

# READ CYCLE
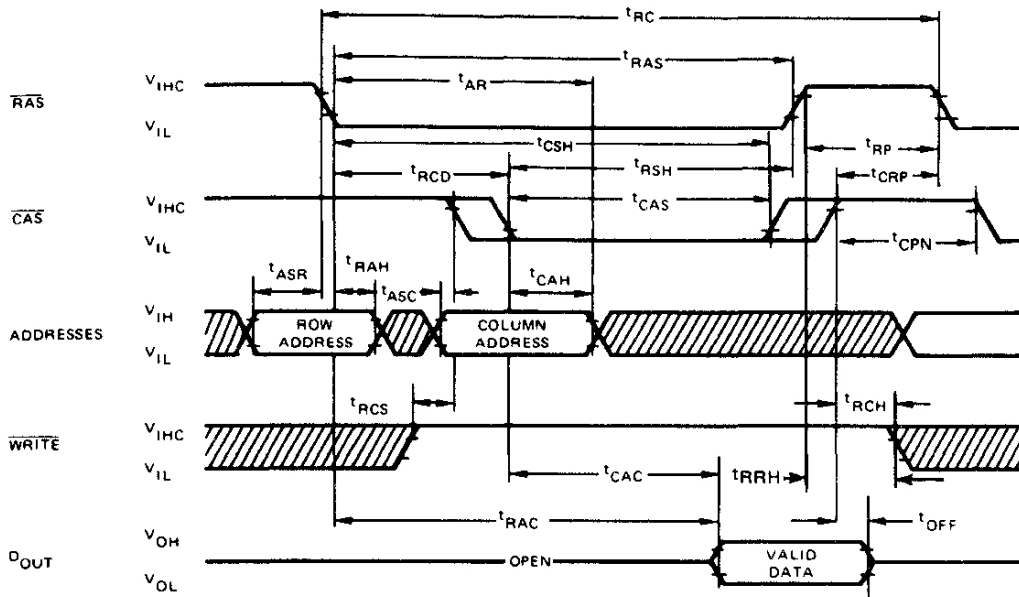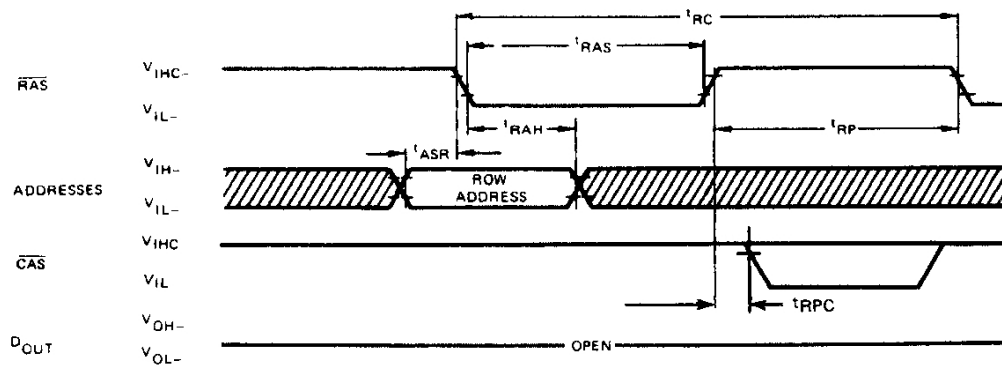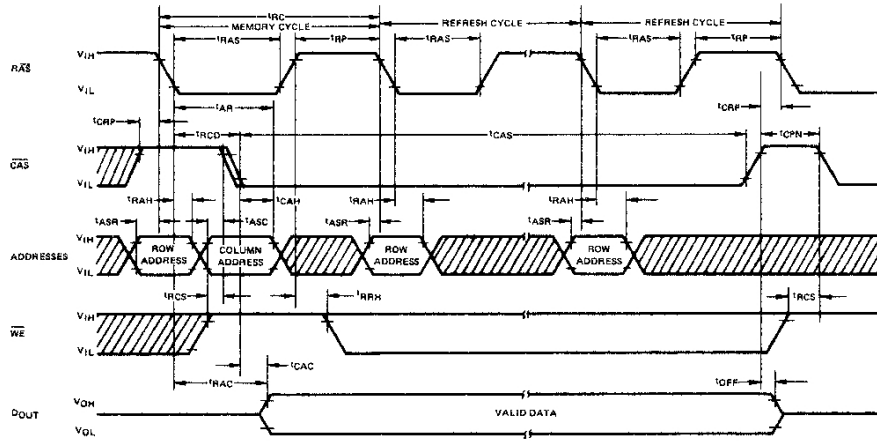


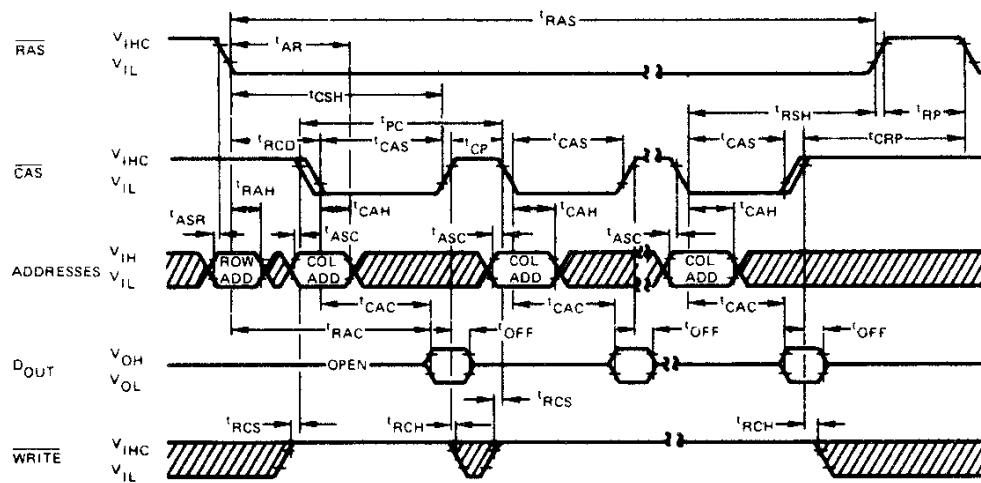# WRITE CYCLE (EARLY WRITE)
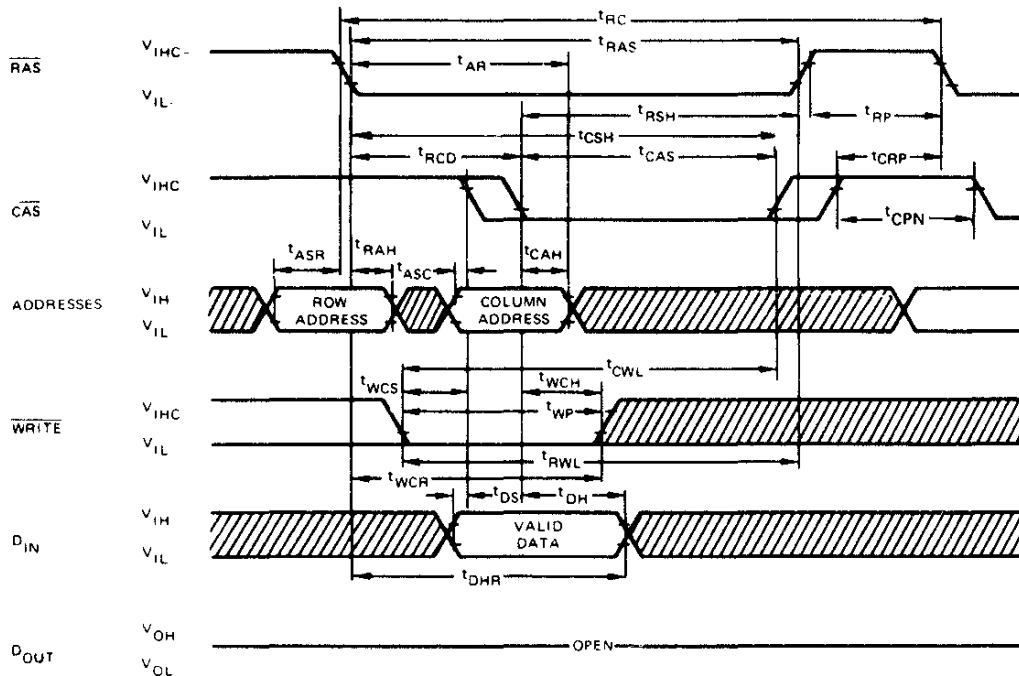


# READ-WRITE/READ-MODIFY—WRITE CYCLE

# "RAS-ONLY" REFRESH CYCLE



# HIDDEN REFRESH CYCLE



# PAGE MODE READ CYCLE



# PAGE MODE WRITE CYCLE
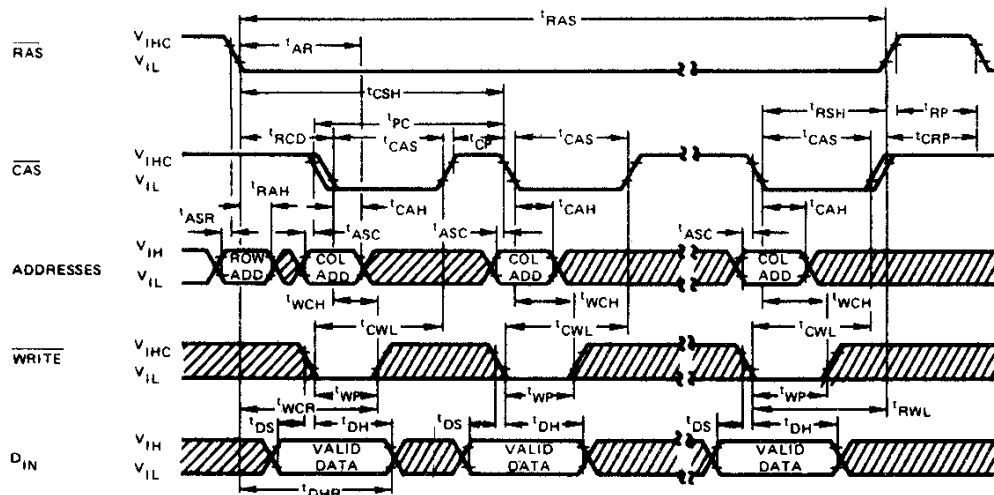
| PARAMETER | SYMBOL | LIMITS | | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| Input Capacitance ($A_0$-$A_7$), $D_{IN}$ | $C_{I1}$ | | 5 | 6 | pF | |
| Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$ | $C_{I2}$ | | | 10 | pF | |
| Output Capacitance ($D_{OUT}$) | $C_0$ | | | 7 | pF | |
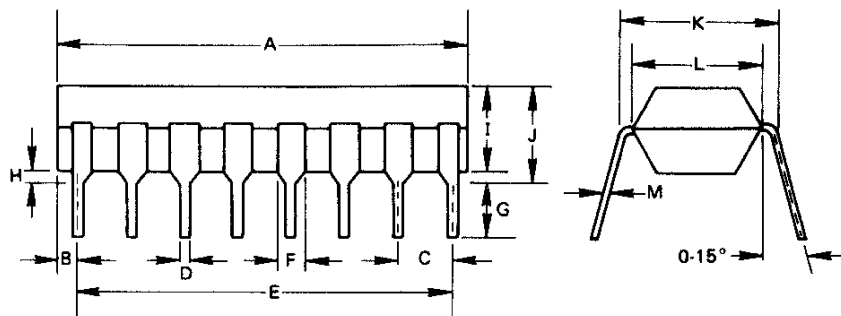


Plastic

μPD4164C

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 19.4 MAX. | 0.76 MAX. |
| B | 0.81 | 0.03 |
| C | 2.54 | 0.10 |
| D | 0.5 | 0.02 |
| E | 17.78 | 0.70 |
| F | 1.3 | 0.051 |
| G | 2.54 MIN. | 0.10 MIN. |
| H | 0.5 MIN. | 0.02 MIN. |
| I | 4.05 MAX. | 0.16 MAX. |
| J | 4.55 MAX. | 0.18 MAX. |
| K | 7.62 | 0.30 |
| L | 6.4 | 0.25 |
| M | $0.25 ^{+0.10}_{-0.05}$ | 0.01 |
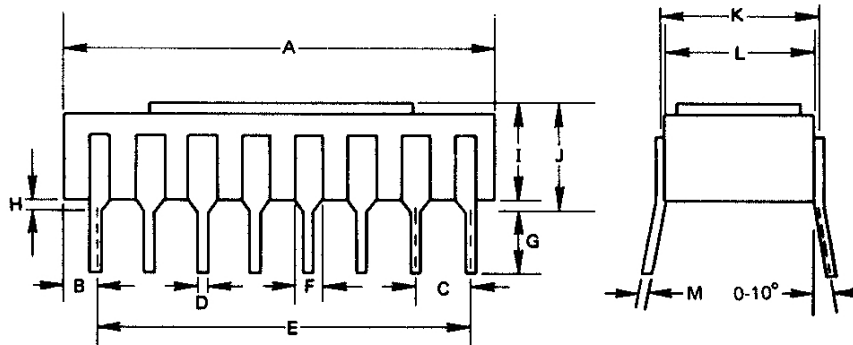


Ceramic

μPD4164D

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 20.5 MAX. | 0.81 MAX. |
| B | 1.36 | 0.05 |
| C | 2.54 | 0.10 |
| D | 0.5 | 0.02 |
| E | 17.78 | 0.70 |
| F | 1.3 | 0.051 |
| G | 3.5 MIN. | 0.14 MIN. |
| H | 0.5 MIN. | 0.02 MIN. |
| I | 4.6 MAX. | 0.18 MAX. |
| J | 5.1 MAX. | 0.20 MAX. |
| K | 7.6 | 0.30 |
| L | 7.3 | 0.29 |
| M | 0.27 | 0.01 |