## Description

The µPD4016 is a 16,384-bit static Random-access Memory device organized as 2,048 words by 8 bits. Using a scaled NMOS technology, its design provides the ease-of-use features associated with nonclocked static memories. The µPD4016 has a three-state output and offers a standby mode with an attendant 75% savings in power consumption. It features equal access and cycle times and provides an output enable function that eliminates the need for external bus buffers. The µPD4016 is packaged in a 600-mil-wide standard 24-pin dual-in-line package which is plug-compatible with 16K EPROMS.

## Features

- [ ] Scaled NMOS technology
- [ ] Completely static memory: no clock, no refresh
- [ ] Equal access and cycle times
- [ ] Single +5V power supply
- [ ] Automatic power-down
- [ ] All inputs and outputs directly TTL-compatible
- [ ] Common I/O capability
- [ ] $\overline{OE}$ eliminates need for external bus buffers
- [ ] Three-state outputs
- [ ] Plug-compatible with 16K 5V EPROMS (600 mil)
- [ ] Low power dissipation in standby mode
- [ ] Available in a standard 24-pin dual-in-line package (600-mil width)
- [ ] 4 performance ranges:

| Device | Access Time | R/W Cycle Time | Power Supply | |
|---|---|---|---|---|
| | | | Active | Standby |
| µPD4016C-1 | 250ns | 250ns | 60mA | 15mA |
| µPD4016C-2 | 200ns | 200ns | 60mA | 15mA |
| µPD4016C-3 | 150ns | 150ns | 60mA | 15mA |
| µPD4016C-5 | 120ns | 120ns | 60mA | 15mA |

## Pin Configuration
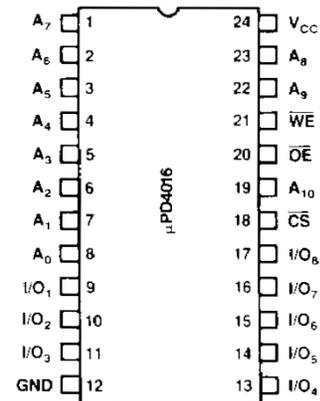


## Pin Identification

| Pin No. | Symbol | Description |
|---|---|---|
| 1-8, 22, 23 | $A_0 - A_{10}$ | Address Inputs |
| 9-11, 13-17 | $I/O_1 - I/O_8$ | Data Input/Output |
| 12 | GND | Ground |
| 18 | $\overline{CS}$ | Chip Select |
| 20 | $\overline{OE}$ | Output Enable |
| 21 | $\overline{WE}$ | Write Enable |
| 24 | $V_{CC}$ | +5V Power Supply |

## Truth Table

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | I/O | Power |
|---|---|---|---|---|---|
| H | X | X | Not Selected | High-Z | Standby |
| L | L | H | Read | $D_{OUT}$ | Active |
| L | H | L | Write | $D_{IN}$ | Active |
| L | L | L | Write | $D_{IN}$ | Active |

## Absolute Maximum Ratings*

| | |
|---|---|
| Temperature Under Bias | -10°C to +85°C |
| Storage Temperature, $T_{ST}$ | -55°C to +125°C |
| Voltage on any Pin with Respect to Ground | -1.5V to +7V |
| DC Output Current, $I_O$ | 20mA |
| Power Dissipation, $P_D$ | 1W |

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# Block Diagram
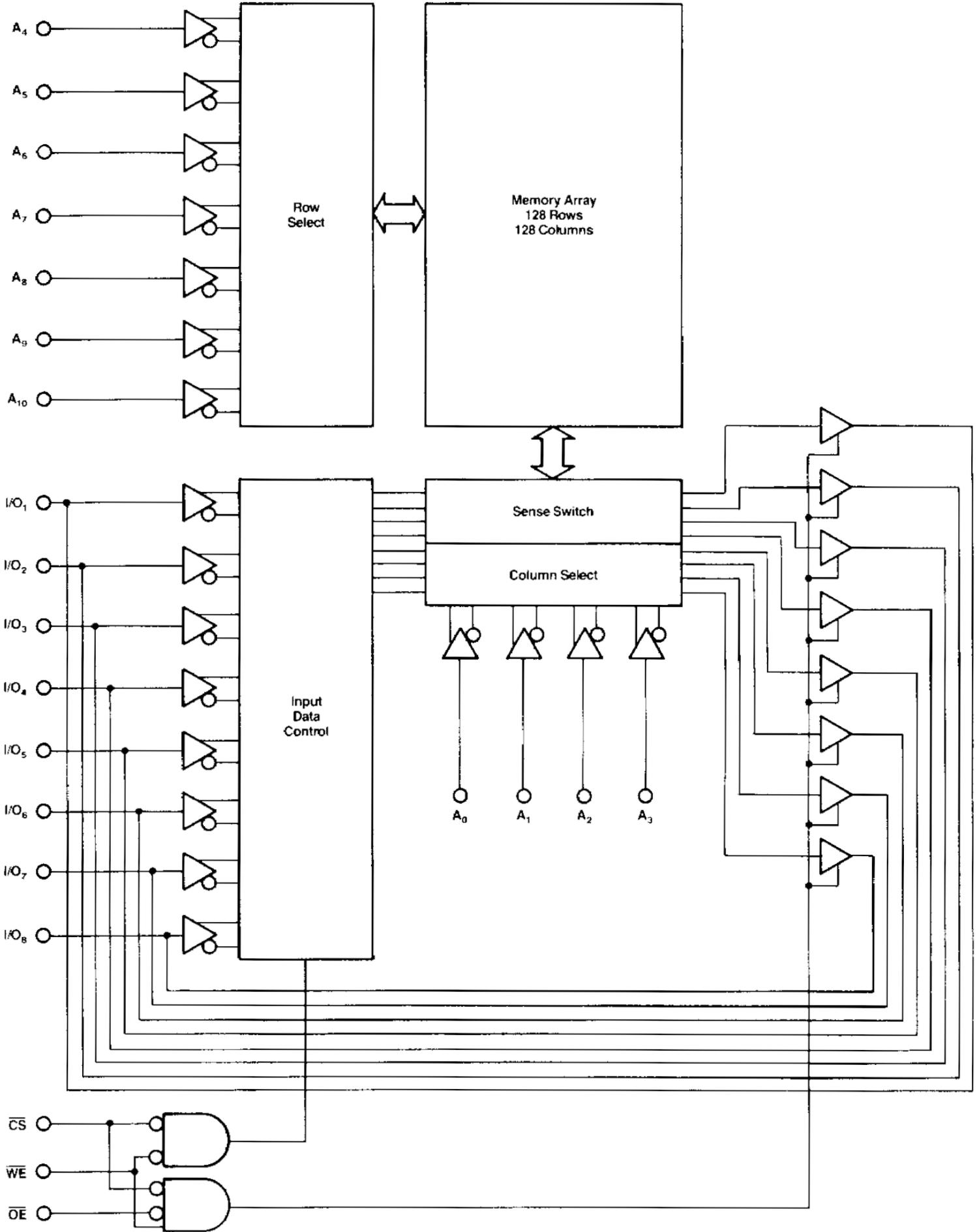
## Capacitance ①

$T_A = 25°C; f = 1MHz$

| Parameter | Symbol | Limits Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | | 5 | pF | $V_{IN} = 0V$ |
| I/O Capacitance | $C_{IO}$ | | | 7 | pF | $V_{IO} = 0V$ |

**Note:** ① This parameter is sampled and not 100% tested.

## DC Characteristics

$T_A = 0°C to +70°C; V_{CC} = 5V ± 10\%$

| Parameter | Symbol | Limits Min | Typ | Max | Unit | Test Conditions ① |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | | | 10 | μA | $V_{CC}$ = Max<br>$V_{IN}$ = GND to $V_{CC}$ |
| Output Leakage Current | $I_{LO}$ | | | 10 | μA | $V_{CC}$ = Max; $\overline{CS}$ = $V_{IH}$<br>$V_{OUT}$ = GND to $V_{CC}$ |
| Operating Current | $I_{CC}$ | | | 60 | mA | $V_{CC}$ = Max; $\overline{CS}$ = $V_{IL}$<br>(outputs open) |
| Standby Current | $I_{SB}$ | | | 15 | mA | $V_{CC}$ = Min to Max;<br>$\overline{CS}$ = $V_{IH}$ |
| Input Low Voltage | $V_{IL}$ | −1.5 | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | 6.0 | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 4mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = 1mA |
| Output Short-circuit Current | $I_{OS}$ | | 70 | | mA | $V_{OUT}$ = GND to $V_{CC}$ |

**Note:** ① Input pulse levels: 0.8V to 2.2V
Input rise and fall times: 10ns
Input timing reference levels: 1.5V
Output timing reference levels: 1.5V

*Figure 1. Loading Conditions Test Circuit*
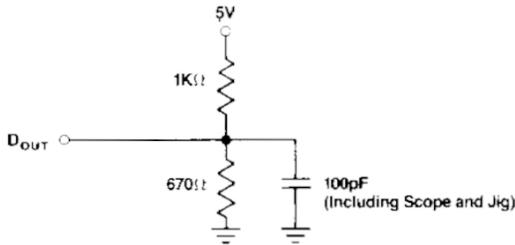


*Figure 2. Input Pulse Test Circuit*
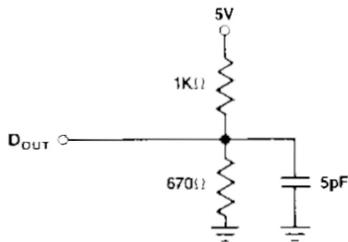


## AC Characteristics

$T_A = 0°C to +70°C; V_{CC} = 5V ± 10\%$

### Read Cycle

| Parameter | Symbol | Limits ① 4016-5 Min | 4016-5 Max | 4016-3 Min | 4016-3 Max | 4016-2 Min | 4016-2 Max | 4016-1 Min | 4016-1 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 120 | | 150 | | 200 | | 250 | | ns | ② |
| Address Access Time | $t_{AA}$ | | 120 | | 150 | | 200 | | 250 | ns | |
| Chip Select Access Time | $t_{ACS}$ | | 120 | | 150 | | 200 | | 250 | ns | ③ |
| Output Hold from Address Change | $t_{OH}$ | 10 | | 10 | | 10 | | 10 | | ns | |
| Chip Selection to Output in Low-Z | $t_{LZ}$ | 10 | | 10 | | 10 | | 10 | | ns | ④ ⑤ |
| Chip Deselection to Output in High-Z | $t_{HZ}$ | | 45 | | 50 | | 60 | | 80 | ns | ④ ⑤ |
| Output Enable to Output Valid | $t_{OE}$ | | 50 | | 70 | | 90 | | 110 | ns | |
| Output Enable to Output in Low-Z | $t_{OLZ}$ | 10 | | 10 | | 10 | | 10 | | ns | ④ ⑤ |
| Output Disable to Output in High-Z | $t_{OHZ}$ | | 45 | | 50 | | 60 | | 80 | ns | ④ ⑤ |
| Chip Selection to Power-up Time | $t_{PU}$ | 0 | | 0 | | 0 | | 0 | | ns | ⑤ |
| Chip Deselection to Power-down Time | $t_{PD}$ | | 60 | | 70 | | 90 | | 110 | ns | ⑤ |

### Write Cycle

| Parameter | Symbol | Limits ① 4016-5 Min | 4016-5 Max | 4016-3 Min | 4016-3 Max | 4016-2 Min | 4016-2 Max | 4016-1 Min | 4016-1 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Write Cycle Time | $t_{WC}$ | 120 | | 150 | | 200 | | 250 | | ns | |
| Chip Selection to End of Write | $t_{CW}$ | 90 | | 120 | | 160 | | 200 | | ns | |
| Address Valid to End of Write | $t_{AW}$ | 80 | | 90 | | 120 | | 150 | | ns | |
| Address Set-up Time | $t_{AS}$ | 0 | | 0 | | 0 | | 0 | | ns | |
| Write Pulse Width | $t_{WP}$ | 70 | | 80 | | 100 | | 130 | | ns | ⑥ |
| Write Recovery Time | $t_{WR}$ | 10 | | 10 | | 10 | | 10 | | ns | |
| Data Valid to End of Write | $t_{DW}$ | 45 | | 50 | | 60 | | 80 | | ns | |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | 0 | | 0 | | ns | |
| Write Enabled to Output in High-Z | $t_{WZ}$ | | 45 | | 50 | | 60 | | 80 | ns | ⑤ ⑦ |
| Output Active from End of Write | $t_{OW}$ | 10 | | 10 | | 10 | | 10 | | ns | ⑤ ⑦ |

**Notes:** ① See Part No. Package Width table below.
② All read cycle timings are referenced from the last valid address to the first transition address.
③ Address valid prior to or coincident with $\overline{CS}$ transition low.
④ Transition is measured ± 200mV from steady-state voltage with specified load of Figure 1.
⑤ This parameter is sampled and not 100% tested.
⑥ If $\overline{CS}$ and $\overline{OE}$ are both low before write enabled, $t_{WP}$, $t_{WZ}$, $t_{DW}$.
⑦ Transition is measured ± 200mV from steady-state voltage with specified load of Figure 2.

# Timing Waveforms

## Write Cycle No. 1 (WE Controlled)

Address

CS

WE

Data-in

Data-out

$t_{WC}$

$t_{CW}$

$t_{AS}$  $t_{WP}$  $t_{WR}$

$t_{DW}$  $t_{DH}$

$t_{WZ}$  $t_{OW}$  $t_{OH}$

Data Undefined  High Impedance

OE
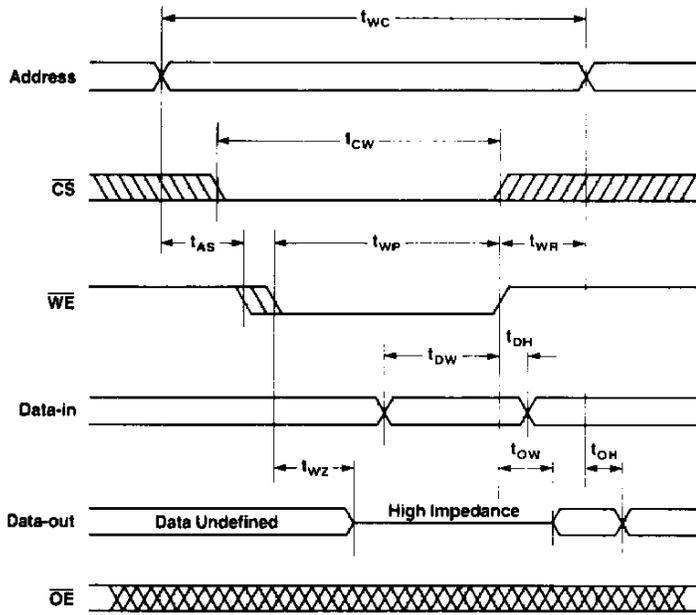
## Write Cycle No. 2 (CS Controlled)

Address

CS

WE

Data-in

Data-out

$t_{WC}$

$t_{AS}$  $t_{CW}$

$t_{AW}$  $t_{WR}$

$t_{WP}$

$t_{DW}$  $t_{DH}$

$t_{LZ}$  $t_{WZ}$

Data Undefined  High Impedance

OE

## Read Cycle No. 1 ① ② ③

Address

Data-out

$t_{RC}$

$t_{AA}$

$t_{OH}$

## Read Cycle No. 2 ① ③ ④

CS

Data-out

$t_{RC}$

$t_{ACS}$  $t_{HZ}$

$t_{LZ}$

$t_{PU}$  $t_{PO}$

$I_{CC}$  $I_{SB}$  50%  50%

## Read Cycle No. 3 ① ②

Address

OE

Data-out

$t_{RC}$

$t_{AA}$

$t_{OE}$  $t_{OHZ}$

$t_{OLZ}$
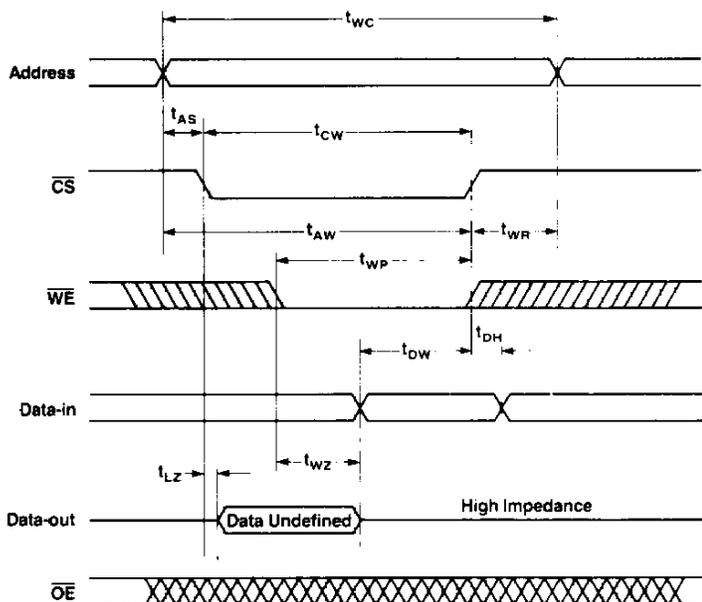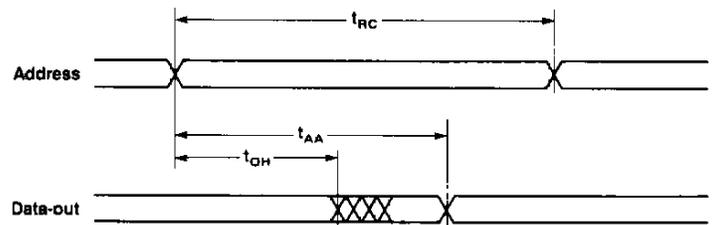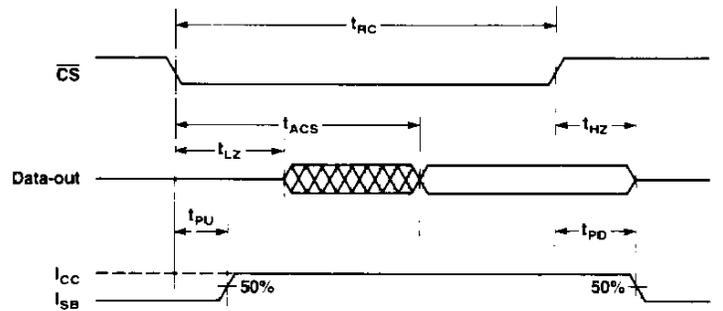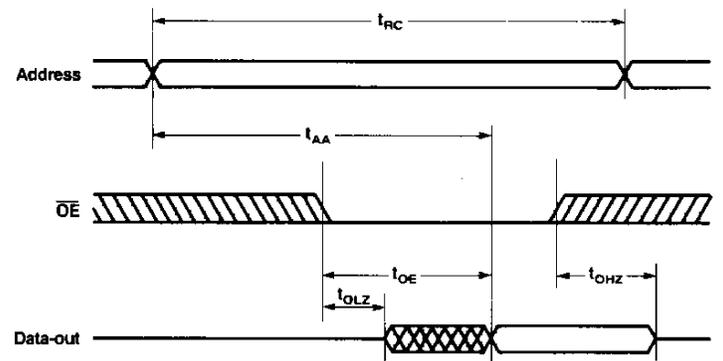
**Notes:** ① WE is high for read cycles.
② Device is continuously selected, CS = $V_{IL}$.
③ OE = $V_{IL}$.
④ Address valid prior to or coincident with CS transition low.