NEC
NEC Electronics Inc.

μPD2764
8,192 x 8-BIT
NMOS UV/OTP EPROM

Description

The μPD2764 is a 65,536-bit (8,192 × 8-bit) electrically programmable read-only memory (EPROM). It operates from a single +5V supply making it ideal for microprocessor applications. It features an output enable control and offers a standby mode with reduction in power consumption.

A distinctive feature of the μPD2764 is a separate output enable control ($\overline{OE}$) in addition to the chip enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple-bus microprocessor systems. The μPD2764 features conventional, simple one-pulse programming controlled by TTL-level signals as well as a high-speed programming mode. Total programming time for all 65,536 bits is 420 seconds for conventional mode, and typically 60 to 120 seconds for the high-speed mode.

The μPD2764 is available in a cerdip package with a quartz window as an ultraviolet (UV), erasable EPROM, or in a plastic package as a one-time-programmable (OTP), non-erasable EPROM.

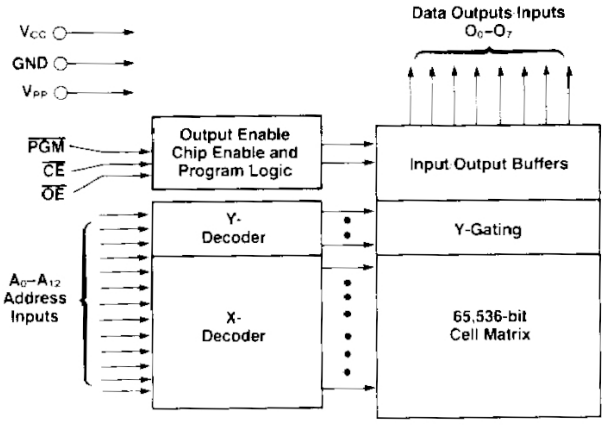
Features

- ☐ Ultraviolet erasable and electrically programmable
- ☐ Access time—200ns max
- ☐ Low power dissipation: 80mA max (active)
  25mA max (standby)
- ☐ High-speed programming mode
  (typical program time 60s to 120s)
- ☐ Programmable with single pulse
  (total program time 420s)
- ☐ Industry standard pinout (JEDEC approved)
- ☐ 4 performance ranges

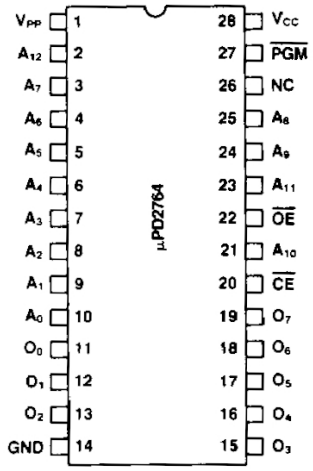
Device	Max Access Time	Max V_{CC} Supply Current	
		Active	Standby
μPD2764-2	200ns	80mA	25mA
μPD2764①	250ns	80mA	25mA
μPD2764-3①	300ns	80mA	25mA
μPD2764-4①	450ns	80mA	25mA

Note: ① Available as either UV or OTP.

Block Diagram



Pin Configuration



Pin Identification

A_0–A_{12}	Addresses
$\overline{OE}$	Output Enable
O_0–O_7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{PGM}$	Program
NC	No Connect

Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z

Note: X can be either V_{IL} or V_{IH}.

Absolute Maximum Ratings*

Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +125°C
Output Voltage	−0.6V to +6.5V
Input Voltage	−0.6V to +6.5V
Supply Voltage V_{CC}	−0.6V to +6.5V
Supply Voltage V_{PP}	−0.6V to +22V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Read Mode and Standby Mode

T_A = 0°C to + 70°C; V_{CC} = +5V ± 5%; V_{PP} = V_{CC}

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1mA
Input High Voltage	V_{IH}	2.0		V_{CC} + 1	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Output Leakage Current	I_{LO}			10	μA	V_{OUT} = 5.25V
Input Leakage Current	I_{LI}			10	μA	V_{IN} = 5.25V
V_{CC} Current Standby	I_{CC1}			25	mA	$\overline{CE}$ = V_{IH}
V_{CC} Current Active	I_{CC2}			80	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{PP} Current	I_{PP1}			15	mA	V_{PP} = 5.25V

Note: V_{PP} may be connected directly to V_{CC} except during programming.

Program, Program Verify, and Program Inhibit Modes

T_A = 25°C ± 5°C; V_{CC}* = +5V ± 5%; V_{PP} = + 21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0		V_{CC} + 1	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1mA
V_{CC} Current	I_{CC2}			100	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

*V_{CC} 6V ± 5% for high-speed programming.

AC Characteristics

Read Mode and Standby Mode

T_A = 0°C to +70°C; V_{CC} = +5V ± 5%

Parameter	Symbol	Limits 2764-2 Min	2764-2 Max	2764① Min	2764① Max	2764-3① Min	2764-3① Max	2764-4① Min	2764-4① Max	Unit	Test Conditions
Address to Output Delay	t_{ACC}		200		250		300		450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		200		250		300		450	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$/V_{PP} to Data Output Delay	t_{OE}		70		100		120		120	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$/V_{PP} to Data Output Float Delay	t_{DF}	0	60	0	85	0	105	0	105	ns	$\overline{CE}$ = V_{IL}
Address to Output Hold Time	t_{OH}	0		0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: ① Available as either UV or OTP.

Test Conditions—
Output Load: 1TTL gate and C_L = 100pF
Input Rise and Fall Times: 20ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Levels:
Inputs: 1.0V and 2.0V
Outputs: 0.8V and 2.0V

Program, Program Verify, and Program Inhibit Modes

T_A = 25°C ± 5°C; V_{CC}* = +5V ± 5%; V_{PP} = +21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2			μs	Input Pulse Levels = 0.8V to 2.2V Input Timing Reference Level = 1.0V and 2.0V Output Timing Reference Level = 0.8V and 2V Input Rise and Fall Times: 20ns
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	0			μs	
$\overline{CE}$ Setup Time	t_{CES}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Chip Enable to Output Float Delay	t_{DF}	0		130	ns	
Data Valid from $\overline{OE}$	t_{OE}			150	ns	
Program Pulse Width*	t_{PW}	45	50	55	ms	
V_{PP} Setup Time	t_{VS}	2			μs	

*V_{CC} = 6V ± 5% and t_{PW} = 1 ms ± 5% for high-speed programming.

Capacitance

T_A = 25°C; f = 1MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}		4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	14	pF	V_{OUT} = 0V

Function

The μPD2764 operates from a single +5V power supply making it ideal for microprocessor applications.

The μPD2764 features a standby mode which reduces the power dissipation.

Operation

The five operation modes of the μPD2764 are listed in Table 1. In the read mode the only power supply required is a +5V supply. During programming all inputs are TTL levels except for V_{PP} which rises from V_{CC} level to 21V.

Read Mode

When $\overline{CE}$ and $\overline{OE}$ are at a low (0) level, Read is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

Standby Mode

The μPD2764 is placed in a standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input. The active power dissipation is also reduced.

Programming Modes

The μPD2764 can be programmed in two ways: (1) conventional programming mode, and (2) high-speed programming mode. In the conventional mode, basically a 50ms $\overline{PGM}$ pulse is applied to each bit location. The high-speed programming mode is similar to the Intelligent Programming Algorithm™, in which up to fifteen 1ms $\overline{PGM}$ pulses are applied to each bit location, followed by an additional 4ms $\overline{PGM}$ pulse for each number of 1ms pulse applied before. The high-speed programming mode reduces the programming time to 60s to 120s typical.

Conventional Programming Mode

Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD2764 is placed in the programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ and $\overline{PGM}$ inputs with V_{PP} at +21V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially, or at random.

When multiple μPD2764s are connected in parallel except for $\overline{CE}$, individual μPD2764s can be programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ input of the desired μPD2764 to be programmed.

Programming of multiple μPD2764s in parallel with the same data is easily accomplished. All the like inputs are tied together and programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ inputs.

High-speed Programming Mode

In this mode, programming begins by addressing the first location, and applying valid data to the eight output pins (a low level TTL signal, 0, into the chosen bit location).

V_{CC} is then raised to 6V ± 0.25V followed by V_{PP} raised to 21V ± 0.5V. A $\overline{PGM}$ pulse of 1ms ± 5% is then applied in the same manner as described in the program mode timing diagram. The bit is then verified and a program/no program decision is made. If the bit is not programmed, another 1ms $\overline{PGM}$ pulse is applied, to a maximum of fifteen times. If the bit gets programmed within fifteen efforts, another pulse of 4ms for each effort is applied and the next address is applied. If the bit does not get programmed in fifteen 1ms efforts, another $\overline{PGM}$ pulse of 60ms is applied and the bit verified. If the bit is not programmed at this stage, the device would be rejected as a program failure. If the bit is programmed, the next address is applied until all addresses are complete.

At this stage, V_{CC} and V_{PP} pins are lowered to 5V ± 5% and all bytes are then verified again for programming.

Program Verify Mode

A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}$ at low (0) levels and $\overline{PGM}$ at a high (1) level.

Programming Inhibit Mode

Programming multiple μPD2764s in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$ (or $\overline{PGM}$) all like inputs (including $\overline{OE}$) of the parallel μPD2764s may be common. Programming is accomplished by applying a low (0) TTL-level program pulse to the $\overline{CE}$ and $\overline{PGM}$ inputs with V_{PP} at +21V. A high (1) level applied to the $\overline{CE}$ (or $\overline{PGM}$) of the other μPD2764 will inhibit it from being programmed.

Output Disable

The data outputs of two or more μPD2764s may be wire-ORed together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD2764s should be disabled by raising the $\overline{CE}$ input to a TTL high. $\overline{OE}$ input should be made common to all devices and connected to the read line from the system control bus. These connections offer the lowest average power consumption.

Erasure Mode

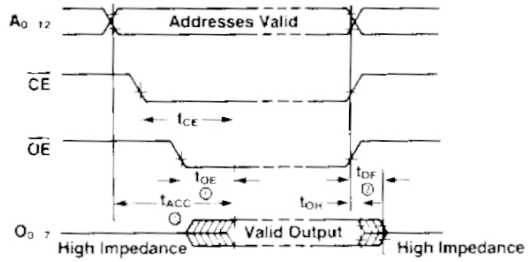
Erasure of the μPD2764 programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 Angstroms (Å). It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD2764. Consequently, if the μPD2764 is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure. Opaque labels are supplied with every device.

The recommended erasure procedure for the μPD2764 is exposure to ultraviolet light with wavelengths of 2,537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be not less than 15W-sec/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12,000μW/cm^2 power rating.

During erasure, the μPD2764 should be placed within 1 inch of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Timing Waveforms

Read Mode



Notes: (1) $\overline{OE}$ may be delayed up to t_{ACC} − t_{OE} after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Program Mode