MPEG Audio Decoder

Description

The HD814102 decodes a compressed audio bit stream conformed to ISO/IEC 11172-3:1993 without using any major external electronic parts such as DRAM. The HD814102 inputs the audio bit stream through 1 bit serial port, 8 bit, or 16 bit parallel port. After the HD814102 detects the header bit field from the audio data read into the HD814102, the HD814102 extracts the data for each bit fields specified on MPEG audio specification, then temporarily stores the data into RAMs, which are the bit allocation RAM, the sampling RAM, and the scale factor RAM. On-chip digital signal processor executes the data processing taking out the data from the RAMs or on-chip constant tables, and stores the processing result into output FIFO. The HD814102 outputs the decoded audio information through S/PDIF (consumer version of AES/EBU, IEC958, or EIAJ CP-1201) interface or 16 bit serial DAC interface. On-chip clock divider provides 3 different clocks to the HD814102 or other peripherals such as bit stream demultiplexer, serial DAC, and S/PDIF decoder LSI.

Features

◊ Conforms to ISO/IEC 11172-3:1993 supporting
- layer I and II
- single channel, dual channel, stereo, and joint stereo.
- all incoming bit rates except free format
- outgoing data sampling frequencies of 32kHz, 44.1kHz, and 48kHz.
- CRC
- ancillary data output timing identification

◊ Equips 3 ports for incoming audio data stream
- 1 bit serial port
- 8 bit parallel port
- 16 bit CPU interface port

◊ Equips 3 data interface methods for incoming audio data stream
- continuous SYNC
- direct memory access (DMA) with 16X8 input buffer
- CPU command with 16X8 input buffer

◊ Equips 2 ports for outgoing audio data stream
- S/PDIF port (AES/EBU consumer use)
- 16 bit PCM serial DAC port with 256 times over sampling

◊ Soft mute and de-mute when header detection error

◊ Indicates status read through both independent pins and CPU interface
- frame synchronization in progress
- bit rates
- sampling frequencies
- layers
- de-emphasis
- stereo

◊ On-chip clock divider
- input : 56.448MHz, 49.152MHz, and/or 22.5792MHz etc.
- output : bit rate, processor clock, and sampling clock

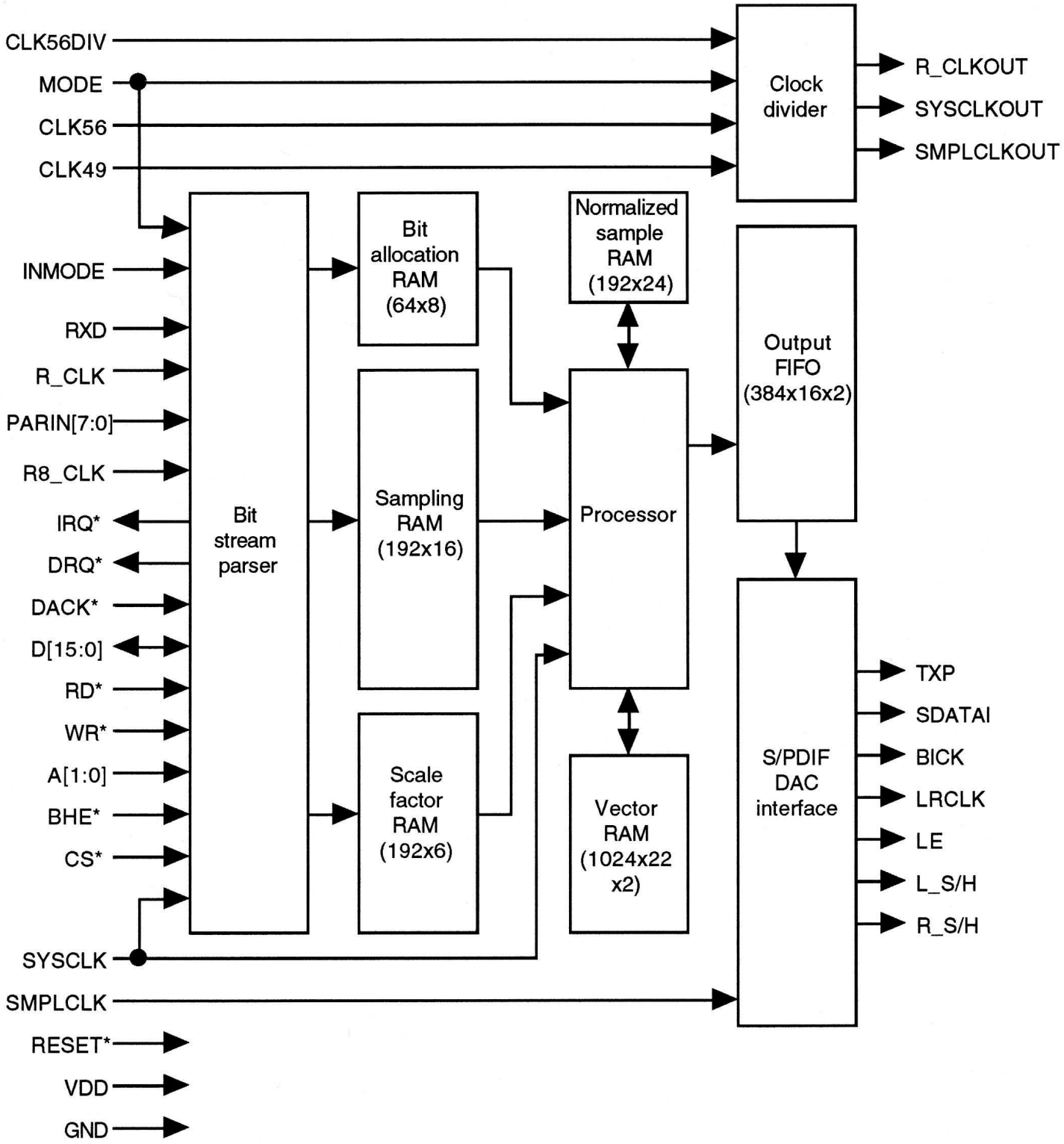
◊ Small scale factor when assembly

◊ 0.8µm 2 layers-Al CMOS technology

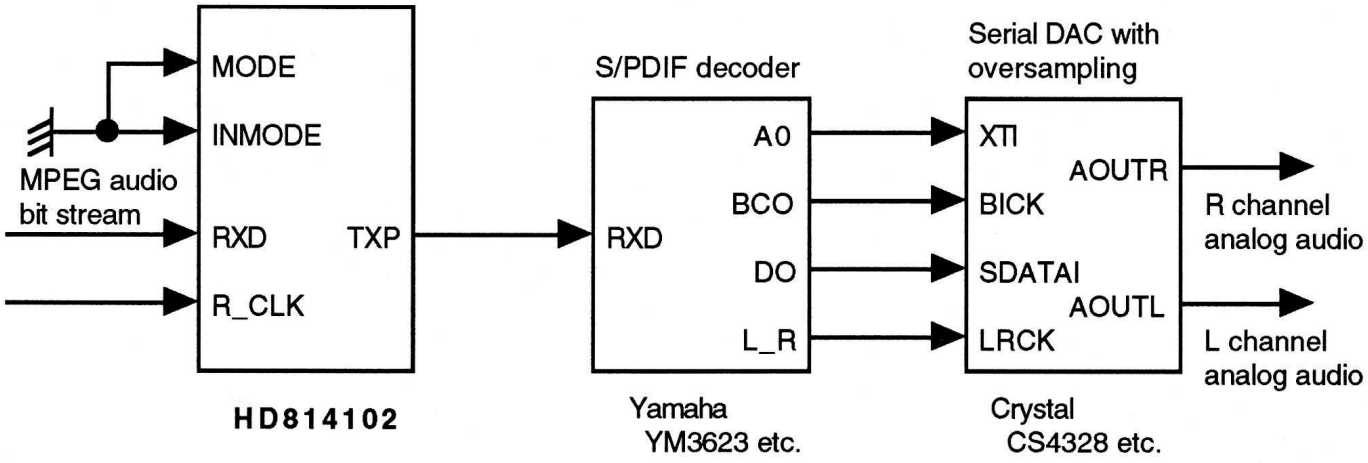
◊ Single +5 volt power supply

◊ Packages: 100 pin PQFP

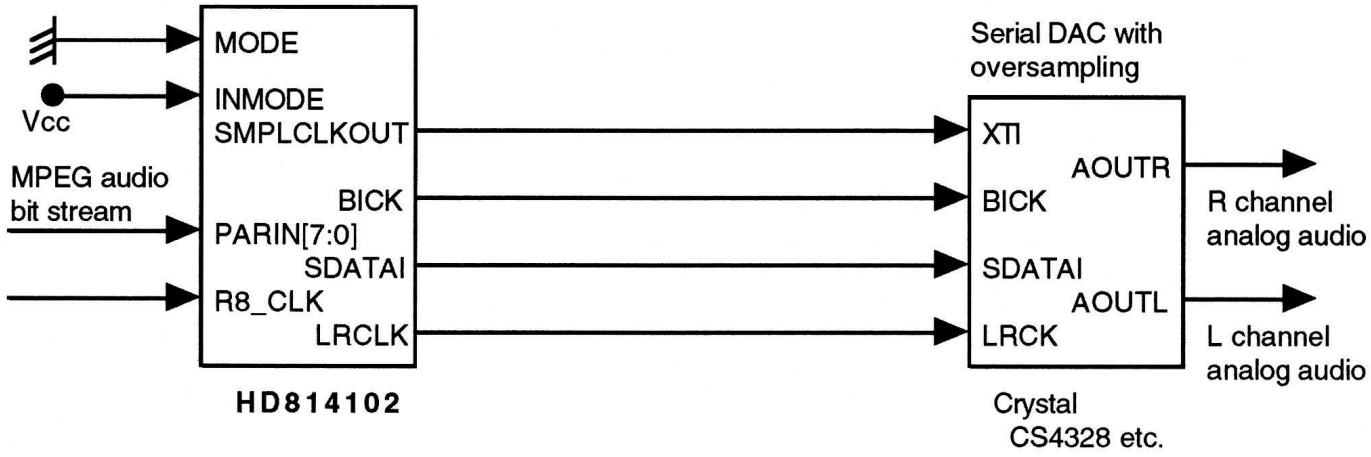
HD814102 Block Diagram



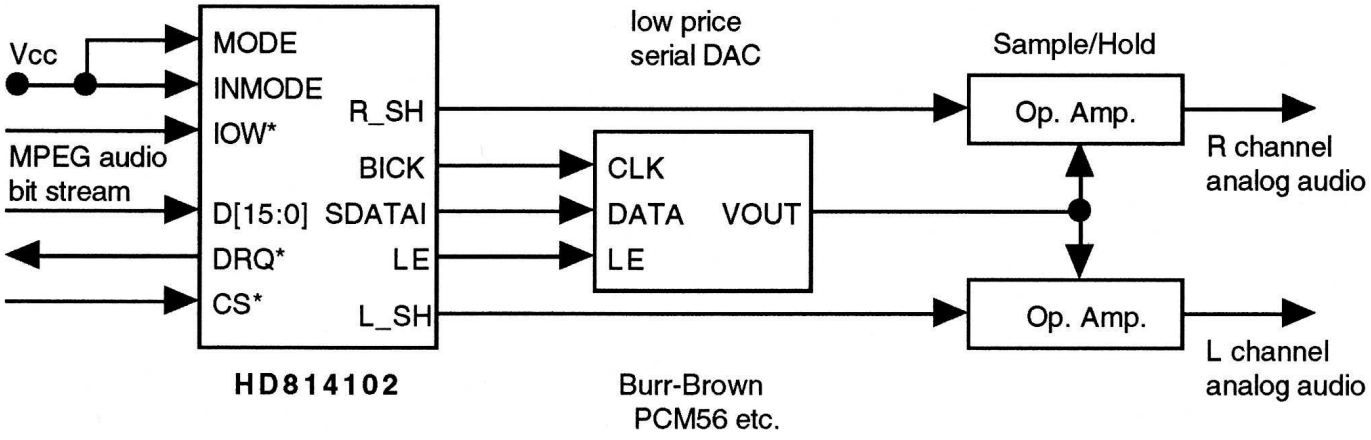
System Configuration Example (Serial-in (SYNC), S/PDIF-out)



System Configuration Example (Parallel-in (SYNC), DAC-1-out)



System Configuration Example (Parallel-in (DMA), DAC-2-out)



Pin Identification

Symbol	I/O	Signal Function
Clock pins		
CLK49	In	When MODE=0 ; Clock supplied to on-chip clock divider. R_CLKOUT, SYSCLKOUT, and SMPLCLKOUT are made when sampling frequency is either 32kHz or 48kHz.. Provide 49.152MHz. When MODE=1 ; Clock supplied to on-chip clock divider. SMPLCLKOUT is made based on the control register contents.
CLK56	In	When MODE=0 ; Clock supplied to on-chip clock divider. R_CLKOUT, SYSCLKOUT, and SMPLCLKOUT are made when sampling frequency is 44.1kHz. Provide 56.448MHz. When MODE=1 ; Clock supplied to on-chip clock divider. SYSCLKOUT and RCLKOUT is made based on CLK56DIV and control register contents.
Incoming data pins		
R_CLK	In	Clock equivalent with bit rate to fetch MPEG audio data stream coming through serial port, RXD.
RXD	In	MPEG audio serial data. Activated when MODE=0 and INMODE=0.
R8_CLK	In	Clock equivalent with 8 times bit rate to fetch MPEG audio data stream coming through 8 bit parallel port, PARIN[7:0].
PARIN[7:0]	In	MPEG audio 8 bit parallel data. Activated when MODE=0 and INMODE=1. PARIN[7] = 1st incoming bit ..... PARIN[0] = 8th incoming bit.
R_CLKOUT	Out	Clock equivalent with bit rate specified by bit rate and layer bit field of MPEG audio data stream.
CPU interface pins		
D[15:0]	In/Out	16 bit data bus. Data shown below can be accessed.
A[1:0]	In	Lower 2 bit address bus.
RD*	In	Read strobe.
WR*	In	Write strobe.
BHE*	In	Together with A0, defines the data access format as shown below. Must be high when 8 bit access.
IRQ*	Out	Interrupt request.
CS*	In	Enables command level access.

MODE	CS*	A1	RD*	WR*	DACK*	Data
1	x	x	1	0	0	Sound data write by DMA
1	0	0	1	0	1	Sound data write by CPU
1	0	1	1	0	1	Control data write by CPU
x	0	1	0	1	1	Status flag read by CPU

A0	BHE*	Data access format
0	0	Even address word
0	1	Even address byte
1	0	Odd address byte
1	1	Odd address byte

Pin Identification (continued)

Symbol	I/O	Signal Function
DMA control pins		
DRQ*	Out	Direct memory access request.
DACK*	In	Indicates DMA transfer is acknowledged and is in progress.
Outgoing data pins		
TXP	Out	Serial bit stream conformed with AES/EBU consumer level (S/PDIF) using bi-phase mark encoding.
SDATAI	Out	16 bit PCM serial data supplied to DAC with serial data input.
SMPLCLKOUT	Out	Clock of 256*fs (sampling frequency)
BICK	Out	Clock of 64 * fs (sampling frequency) supplied to DAC with serial data input.
LRCLK	Out	Indicates either left channel or right channel. Timing signal supplied to DAC with serial data input. High ; left channel. Low ; right channel.
R_SH	Out	Sample/Hold timing signal supplied to operational amplifier of right channel.
L_SH	Out	Sample/Hold timing signal supplied to operational amplifier of left channel.
LE	Out	Latch enable timing signal supplied to DAC with serial data input
SMPLCLK	In	Clock of 256 * fs (sampling frequency) supplied to on-chip S/PDIF and DAC interface logic.
SYSCLKOUT	Out	Clock of CLK49/2 or CLK56/2 when MODE=0. CLK22 when MODE=1.
SYSCLK	In	Clock supplied to on-chip processor.
Operational mode control pins		
SYNCIMM	In	Defines frame synchronization modes. High ; locks frame synchronization soon after the success of header detection. Low ; locks frame synchronization after the success of header detection for continuous 3 frames.
IDVLD	In	Defines if the incoming data is valid or not. High ; valid. Low ; invalid.
LMUTE	In	Defines if the sound of left channel is muted or de-muted. High ; muted. Low ; de-muted.
RMUTE	In	Defines if the sound of right channel is muted or de-muted. High ; muted. Low ; de-muted.
MODE	In	Defines data interface methods High ; CPU interface mode Low ; continuous SYNC mode
CLK56DIV	In	Defines clock divide factor for CLK56. High ; CLK56/2. Low ; CLK56
INMODE	In	Defines SYNCed data input mode. High ; parallel input. Low ; serial input.
ANLGCTRL	In	Defines data flow sequence of SDATAI. High ; LSB first. Low ; MSB first.
SFREQIN[1:0]	In	Defines sampling frequency. Supplied to on-chip clock divider. "00" ; 44.1kHz. "01" ; 48kHz. "10" ; 32kHz. "11" ; invalid.

Pin Identification (continued)

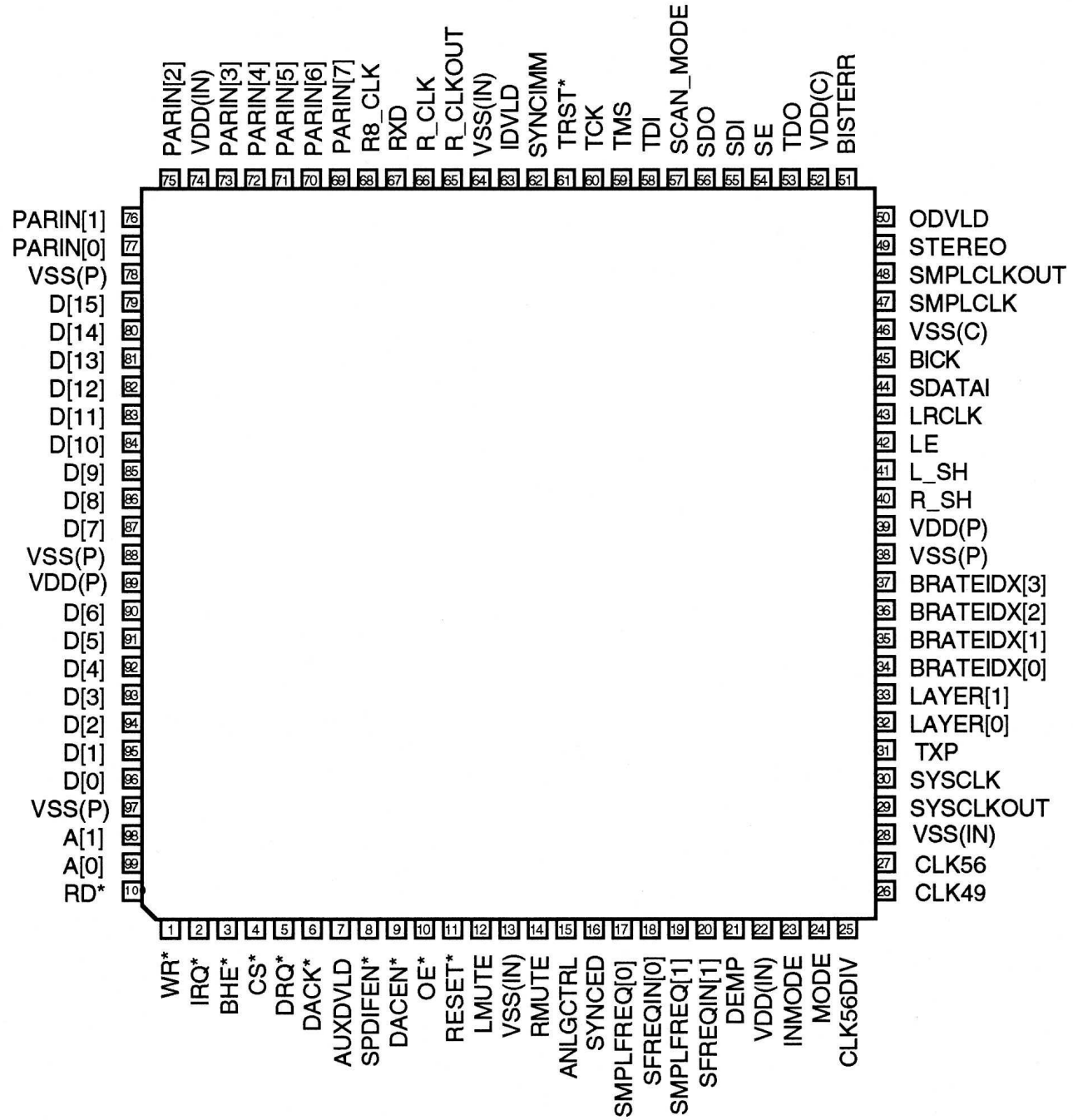
Symbol	I/O	Signal Function
Operational mode control pins (continued)		
RESET*	In	Initializes on-chip logic. High ; normal operation. Low ; initialization.
SPDIFEN*	In	Controls output buffer of TXP. High ; floating. Low ; enabled.
DACEN*	In	Controls output buffers of SDATAI, BICK, LRCLK, DEMP, L_SH, R_SH, and LE. High ; floating. Low ; enabled.
OE*	In	Controls all output buffers. High ; floating. Low ; enabled.
Timing flag pins		
SYNCED	Out	Indicates if the frame synchronization is locked or not. High ; synchronized. Low ; not synchronized.
AUXDVLD	Out	Indicates the timing when ancillary bit is incoming. High ; ancillary bit. Low ; other bit fields.
ODVLD	Out	Indicates if the output data is valid or not. High ; valid. Low ; invalid.
Header decoded result pins		
BRATEIDX[3:0]	Out	Decoded result of bit rate index bit field on the header of MPEG data stream. Incoming data with free format is not available to be decoded. if LAYER[1:0] = "11" (layer I) ; "0000" ; free format. "0001" ; 32kHz. "0010" ; 64kHz. "0011" ; 96kHz. "0100" ; 128kHz. "0101" ; 160kHz. "0110" ; 192kHz. "0111" ; 224kHz. "1000" ; 256kHz. "1001" ; 288kHz. "1010" ; 320kHz. "1011" ; 352kHz. "1100" ; 384kHz. "1101" ; 416kHz. "1110" ; 448kHz. "1111" ; invalid. if LAYER[1:0] = "10" (layer II) ; "0000" ; free format. "0001" ; 32kHz. "0010" ; 48kHz. "0011" ; 56kHz. "0100" ; 64kHz. "0101" ; 80kHz. "0110" ; 96kHz. "0111" ; 112kHz. "1000" ; 128kHz. "1001" ; 160kHz. "1010" ; 192kHz. "1011" ; 224kHz. "1100" ; 256kHz. "1101" ; 320kHz. "1110" ; 384kHz. "1111" ; invalid.
SMPLFRQ[1:0]	Out	Decoded result of sampling frequency bit field of the header. "00" ; 44.1kHz. "01" ; 48kHz. "10" ; 32kHz. "11" ; reserved.
LAYER[1:0]	Out	Decoded result of layer bit field of the header. "00" ; reserved. "01" ; layer III. "10" ; layer II. "11" ; layer I.
DEMP	Out	Decoded result of emphasis bit field of the header. High ; emphasis. Low ; no emphasis.
STEREO	Out	Decoded result of mode bit field of the header. High ; stereophonic. Low ; monaural.

Pin Identification (continued)

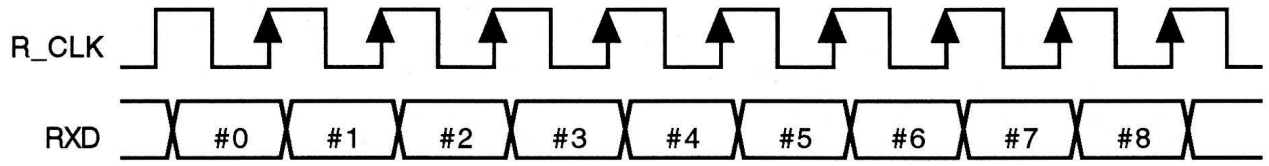
Symbol	I/O	Signal Function
Test pins		
TDI	In	Should be grounded for normal operation. (inputs boundary scan data)
TDO	Out	Should be opened for normal operation. (outputs boundary scan data)
TMS	In	Should be grounded for normal operation. (defines boundary scan test modes)
TCK	In	Should be grounded for normal operation. (clock for boundary scan)
TRST*	In	Should be tied with RESET* for normal operation. (initializes boundary scan logic)
SDI	In	Should be grounded for normal operation. (inputs scan chain data)
SDO	Out	Should be opened for normal operation. (outputs scan chain data)
SCAN_MODE	In	Should be grounded for normal operation. (defines scan chain modes)
SE	In	Should be grounded for normal operation. (defines scan chain modes)
BISTERR	Out	Should be opened for normal operation. (indicates built-in self test error)
Other pins		
VDD		+5 volt power supply
GND		Ground

Pin Configurations

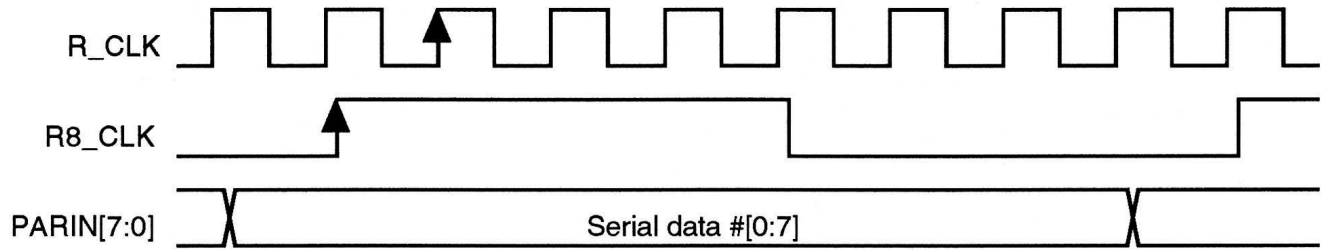
100-pin PQFP



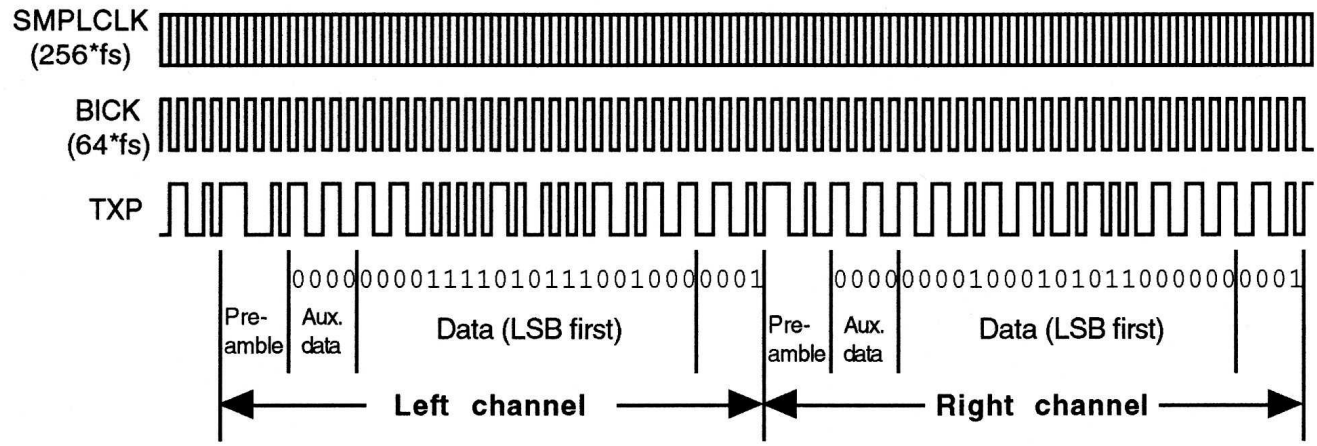
Serial data input timing by continuous SYNC



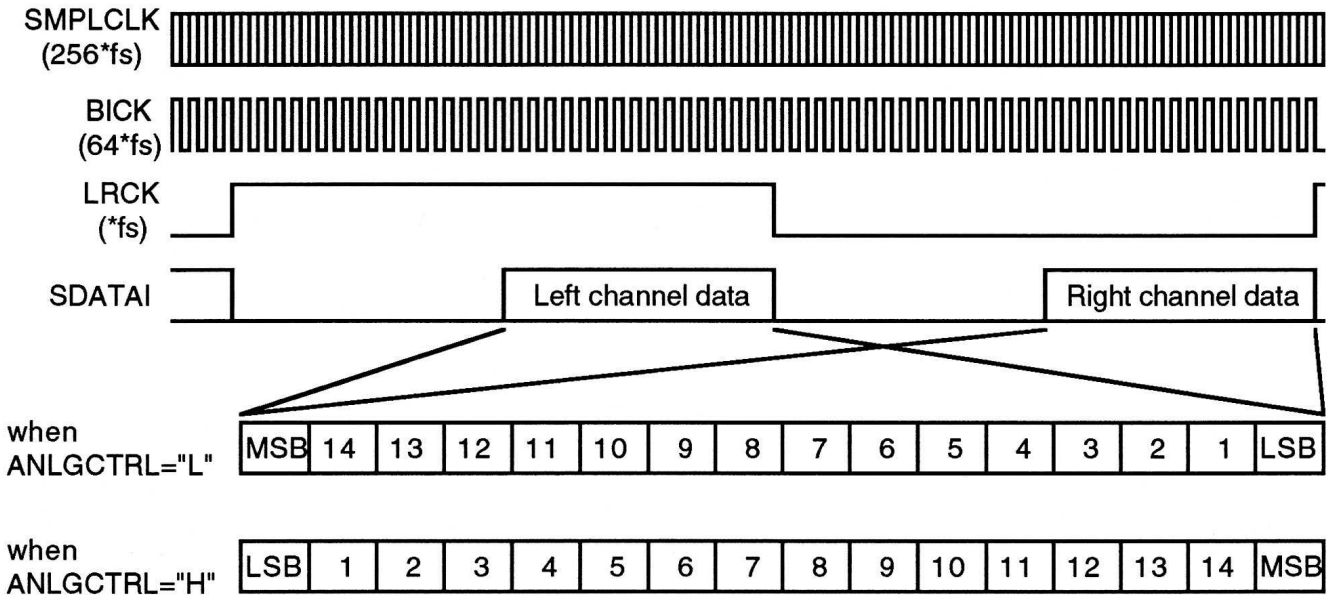
Parallel data input timing by continuous SYNC



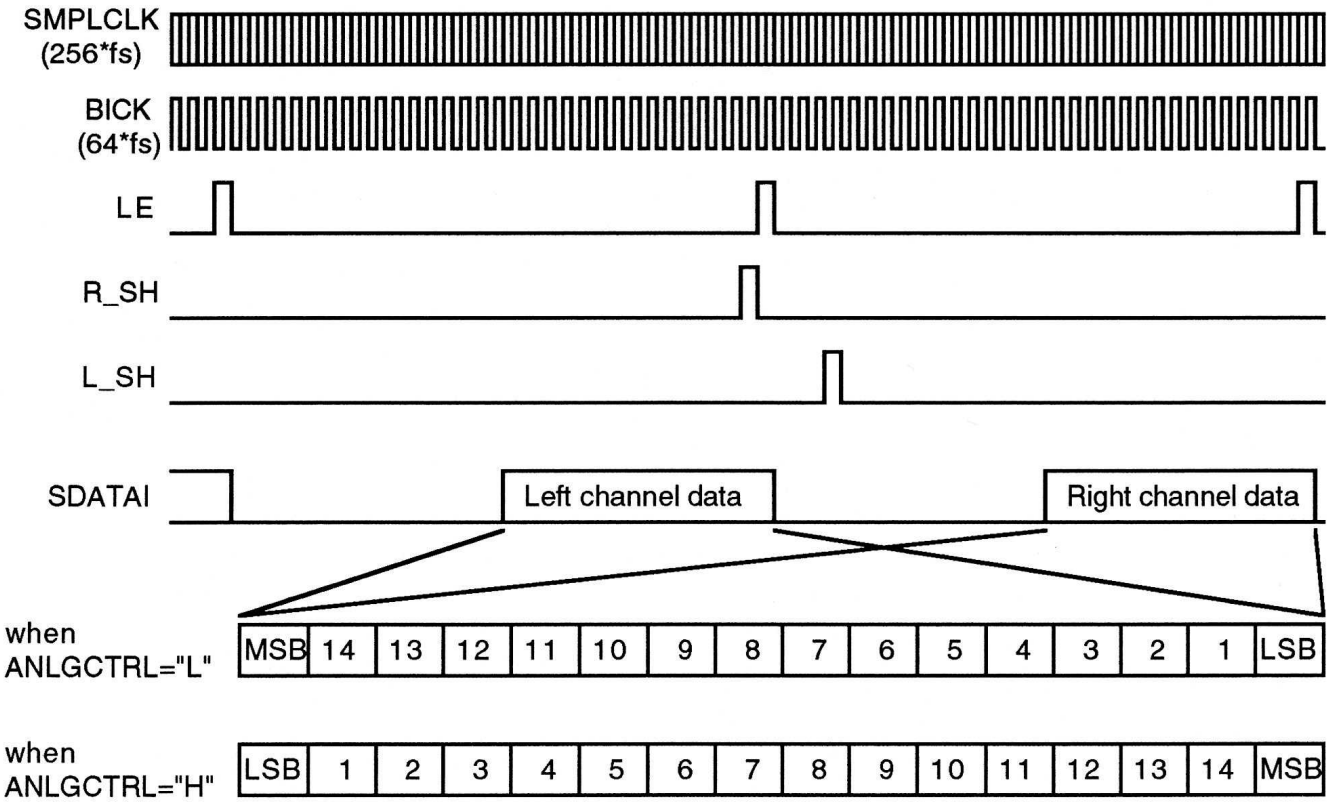
S/PDIF output timing



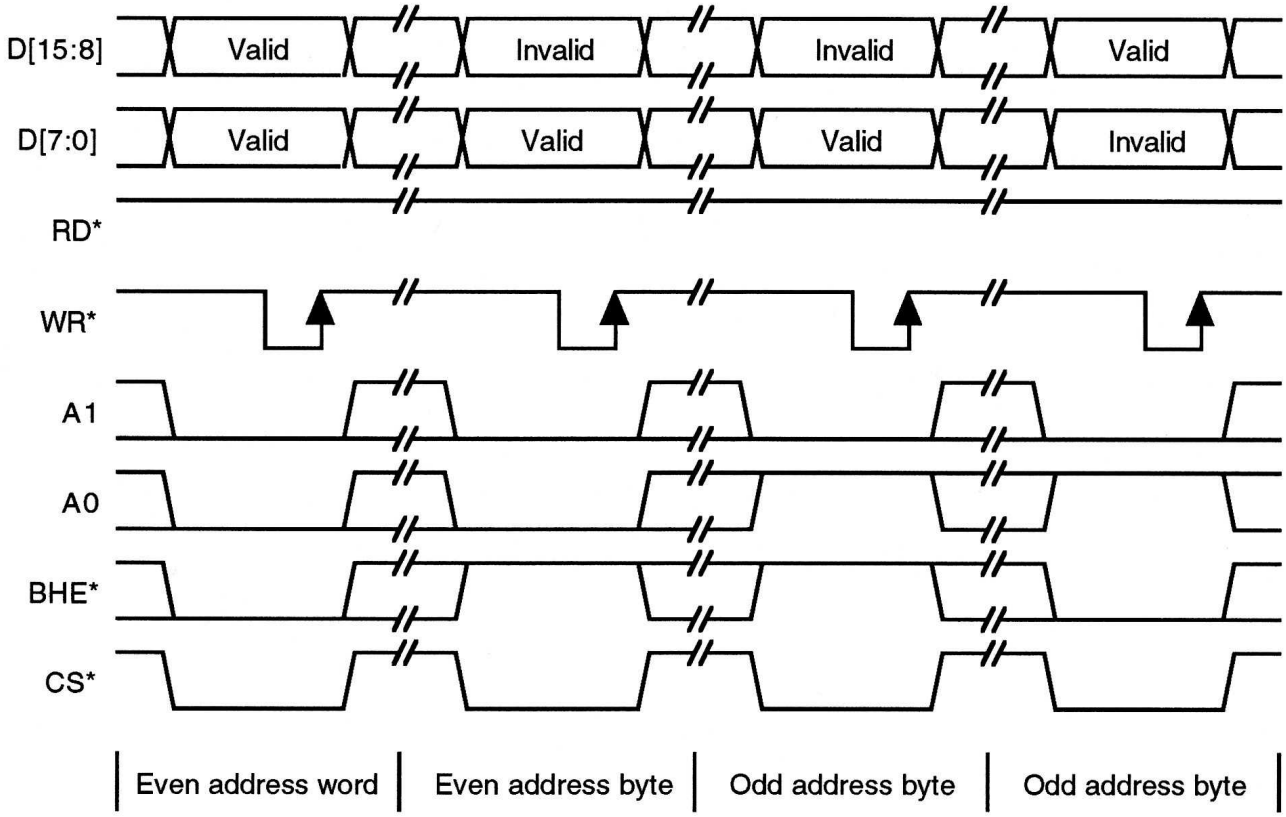
DAC1 output timing



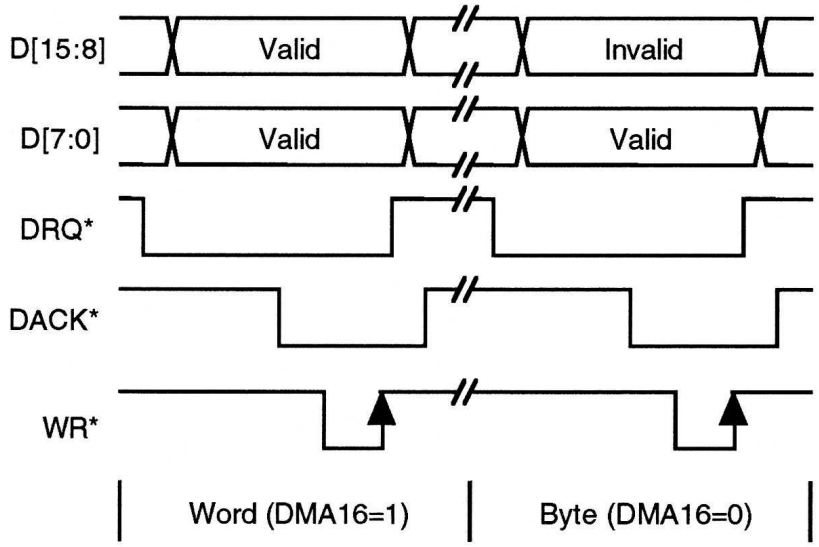
DAC2 output timing



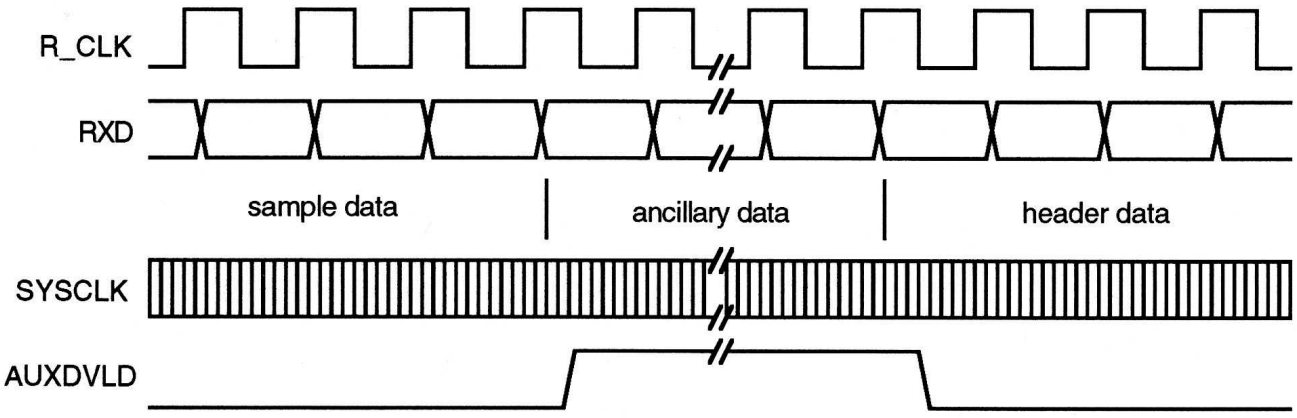
Parallel data input timing by CPU



Parallel data input timing by DMA



AUXDVLD timing



Control register configurations (write only)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
DMA16	SRESET	SFREQIN[1]	SFREQIN[0]	RMUTE	LMUTE	IDVLD	SYNCIMM	A[1:0]=10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
0	C49DIV[1]	0	C49DIV[0]	CLKDIV[3]	CLKDIV[2]	CLKDIV[1]	CLKDIV[0]	A[1:0]=11

When MODE=1, the control register is activated and replaces the corresponding "operational mode control pins" function.
When MODE=0, the control register has no function. The operational mode control pins function.

Symbol	Bit	Register Function (A[1:0]=10) (default=00001111)
DMA16	7	Defines the data width when DMA. High; 16 bit Low ; 8 bit
SRESET	6	Defines if the software reset is forced or not. High ; software reset. Low ; normal use.
SFREQIN[1:0]	5,4	Defines sampling frequency. Supplied to on-chip clock divider. "00" ; 44.1kHz. "01" ; 48kHz. "10" ; 32kHz. "11" ; invalid.
RMUTE	3	Defines if the sound of right channel is muted or de-muted. High ; muted. Low ; de-muted.
LMUTE	2	Defines if the sound of left channel is muted or de-muted. High ; muted. Low ; de-muted.
IDVLD	1	Defines if the incoming data is valid or not. High ; valid. Low ; invalid.
SYNCIMM	0	Defines frame synchronization modes. High ; locks frame synchronization soon after the success of header detection. Low ; locks frame synchronization after the success of header detection for continuous 3 frames.
Symbol	**Bit**	**Register Function (A[1:0]=11) (default=00000111)**
C49DIV	6,4	Defines the clock divide factor for SMPLCLKOUT from CLK49. "00" ; 1 "01" ; 2 "10" ; 3/2 "11" ; 4
CLKDIV[3:0]	3,2,1,0	Defines the clock divide factor N for R_CLKOUT from CLK22 (CLK22/N) except the case shown below. "0000" ; 8 "0001" ; 16 "0010" ; 24 "0011" ; 32 "0100" ; 40 "0101" ; 48 "0110" ; 56 "0111" ; 64 "1000" ; 72 "1001" ; 80 "1010" ; 88 "1011" ; 96 "1100" ; 104 "1101" ; 112 "1110" ; 120 "1111" ; 128

Symbol	Bit	Register Function	(A[1:0]=11)	(default=00000111)	
CLKDIV[3:0]	3,2,1,0	In case of 32k/48kbps.			
		"0000" ; 16	"0001" ; 32	"0010" ; 48	"0011" ; 64
		"0100" ; 80	"0101" ; 96	"0110" ; 112	"0111" ; 128
		"1000" ; 144	"1001" ; 160	"1010" ; 176	"1011" ; 192
		"1100" ; 208	"1101" ; 224	"1110" ; 240	"1111" ; 256

Bit 7 and 5 of control register (A[1:0]=11) are reserved for test use.

Status flag register configurations (read only)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
LAYER[1]	LAYER[0]	SMPLFRQ[1]	SMPLFRQ[0]	BRATEIDX[3]	BRATEIDX[2]	BRATEIDX[1]	BRATEIDX[0]	A[1:0]=10

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
IBFULL	OBFULL	TMPBFULL	DEMP	ODVLD	AUXDVLD	STEREO	SYNCED	A[1:0]=11

The status flag register returns the corresponding "Header decoded result and timing flag pins" signal level.

Symbol	Bit	Register Function (A[1:0]=10)
LAYER[1:0]	7,6	Decoded result of layer bit field of the header. "00" ; reserved. "01" ; layer III. "10" ; layer II. "11" ; layer I.
SMPLFRQ[1:0]	5,4	Decoded result of sampling frequency bit field of the header. "00" ; 44.1kHz. "01" ; 48kHz. "10" ; 32kHz. "11" ; reserved.
BRATEIDX[3:0]	3,2,1,0	Decoded result of bit rate index bit field on the header of MPEG data stream. if LAYER[1:0] = "11" (layer I) ; "0000" ; free format. "0001" ; 32kHz. "0010" ; 64kHz. "0011" ; 96kHz. "0100" ; 128kHz. "0101" ; 160kHz. "0110" ; 192kHz. "0111" ; 224kHz. "1000" ; 256kHz. "1001" ; 288kHz. "1010" ; 320kHz. "1011" ; 352kHz. "1100" ; 384kHz. "1101" ; 416kHz. "1110" ; 448kHz. "1111" ; invalid. if LAYER[1:0] = "10" (layer II) ; "0000" ; free format. "0001" ; 32kHz. "0010" ; 48kHz. "0011" ; 56kHz. "0100" ; 64kHz. "0101" ; 80kHz. "0110" ; 96kHz. "0111" ; 112kHz. "1000" ; 128kHz. "1001" ; 160kHz. "1010" ; 192kHz. "1011" ; 224kHz. "1100" ; 256kHz. "1101" ; 320kHz. "1110" ; 384kHz. "1111" ; invalid.

Symbol	Bit	Register Function (A[1:0]=11)
IBFULL	7	Indicate if data input buffer is full. High ; full Low ; not full
OBFULL	6	Indicate if output buffer is full. High ; full Low ; not full
TMPBFULL	5	Indicates if the temporary buffer on parser is full. High ; full Low ; not full
DEMP	4	Decoded result of emphasis bit field of the header. High ; emphasis. Low ; no emphasis.

Symbol	Bit	Register Function (A[1:0]=11)
ODVLD	3	Indicates if the output data is valid or not. High ; valid. Low ; invalid.
AUXDVLD	2	Indicates the timing when ancillary bit is incoming. High ; ancillary bit. Low ; other bit fields.
STEREO	1	Decoded result of mode bit field of the header. High ; stereophonic. Low ; monaural.
SYNCED	0	Indicates if the frame synchronization is locked or not. High ; synchronized. Low ; not synchronized.

Electrical Specifications

Absolute Maximum Ratings

T_A = +25°C

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_I	-0.5 to +7.0	V
Output Voltage	V_O	-0.5 to +7.0	V
Operating temperature	T_{OPT}	0 to +70	℃
Storage temperature	T_{STG}	-65 to +150	℃
Power dissipation	P_D	750	mW

Capacitance

T_A = +25°C, V_{DD} = GND = 0V

Parameter	Symbol	Min	Max	Unit	Condition
Input	C_I		10	pF	f = 1MHz ;
Output	C_O		20	pF	unmeasured pins
Input/Output	$C_{I/O}$		20	pF	returned to 0V

DC Characteristics

T_A = 0 to +70°C; V_{DD} = +5.0V ± 10%

Parameter	Symbol	Min	Max	Unit	Condition
Low-level input voltage	V_{IL}	-0.5	0.3*V_{DD}	V	
High-level input voltage	V_{IH}	0.7*V_{DD}	V_{DD}+0.5	V	
Low-level output voltage	V_{OL}		0.4	V	I_{OL}=2.2mA
High-level output voltage	V_{OH}	2.4		V	I_{OH}=-400μA
Low-level input leakage current	I_{IL1}	-10	+10	μA	V_I=0; CLK49, CLK56
Low-level input leakage current	I_{IL2}	-200	-10	μA	V_I=0; Except CLK49, CLK56
High-level input leakage current	I_{IH1}	-10	+10	μA	V_I=V_{DD}; CLK49, CLK56
High-level input leakage current	I_{IH2}	-10	+10	μA	V_I=V_{DD}; Except CLK49, CLK56
Low-level output leakage current	I_{OL}		TBD	μA	V_O=0
High-level output leakage current	I_{OH}		TBD	μA	V_O=V_{DD}
Supply current	I_{DD}		100	mA	

AC Characteristics

T_A = 0 to +70°C; V_{DD} = +5.0V ± 10%; see Voltage threshold for timing measurements

Parameter		Symbol	Min	Max	Unit	Condition
Clock						
Clock period	CLK56	t_{CYK}	Typ. = 17.7154		ns	
	CLK49	t_{CYK}	Typ. = 20.345		ns	
	CLK49, CLK56	t_{CYK}	17		ns	
	SYSCLK	t_{CYSK}	34		ns	
	SMPLCLK	t_{CYPK}	80		ns	
	R_CLK	t_{CYRK}	2		µs	
High-level clock width	CLK49, CLK56	t_{WHK}	7		ns	
	SYSCLK	t_{WHSK}	14		ns	
	SMPLCLK	t_{WHPK}	35		ns	
	R_CLK	t_{WHRK}	1		µs	
Low-level clock width	CLK49, CLK56	t_{WLK}	7		ns	
	SYSCLK	t_{WLSK}	14		ns	
	SMPLCLK	t_{WLPK}	35		ns	
	R_CLK	t_{WLRK}	1		µs	
Clock rise time	CLK49, CLK56	t_{RK}		2	ns	
	SYSCLK	t_{RSK}		4	ns	
	SMPLCLK	t_{RPK}		5	ns	
	R_CLK	t_{RRK}		10	ns	
Clock fall time	CLK49, CLK56	t_{FK}		2	ns	
	SYSCLK	t_{FSK}		4	ns	
	SMPLCLK	t_{FPK}		5	ns	
	R_CLK	t_{FRK}		10	ns	
Incoming data						
RXD setup time to R_CLK ↑		t_{SRXRK}	20		ns	
RXD hold time from R_CLK ↑		t_{HRXRK}	5		ns	
R8_CLK setup time to R_CLK ↑		t_{S8KRK}	20		ns	
R8_CLK hold time from R_CLK ↑		t_{H8KRK}	5		ns	
R8_CLK period		t_{CY8K}	Typ. = $8t_{CYRK}$		ns	
R8_CLK width, high		t_{WH8K}	t_{CYRK}-5	$7t_{CYRK}$+5	ns	
R8_CLK width, low		t_{WL8K}	t_{CYRK}-5	$7t_{CYRK}$+5	ns	
PARIN[7:0] setup time to R8_CLK ↑		t_{SPI8K}	20		ns	
PARIN[7:0] hold time from R8_CLK ↑		t_{HPI8K}	5		ns	

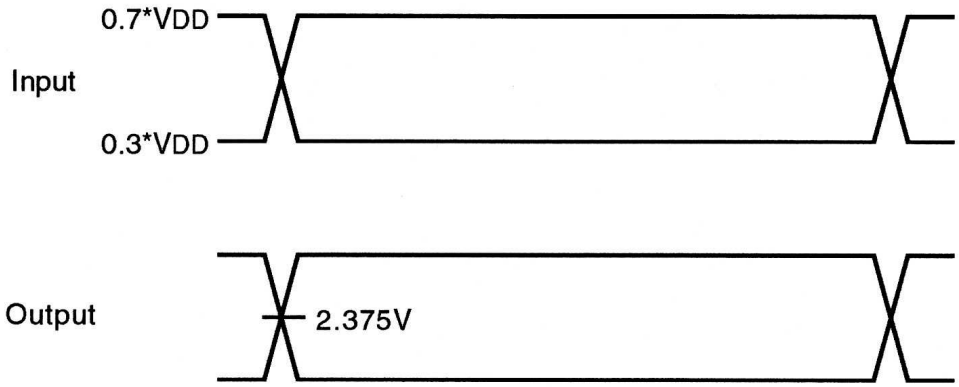
AC Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Condition
Outgoing data					
SMPLCLK ↑ to BICK delay time	t_{DSKBK}		50	ns	C_L = 50pF
BICK period	t_{CYBK}	Typ. = $4t_{CYPK}$		ns	
BICK width, high	t_{WHBK}	$2t_{CYPK}$-5	$2t_{CYPK}$+5	ns	
BICK width, low	t_{WLBK}	$2t_{CYPK}$-5	$2t_{CYPK}$+5	ns	
BICK ↓ to LRCLK delay time	t_{DBKLK}		50	ns	C_L = 50pF
LRCLK period	t_{CYLK}	Typ. = $64t_{CYBK}$		ns	
LRCLK width, high	t_{WHLK}	$32t_{CYBK}$-5	$32t_{CYBK}$+5	ns	
LRCLK width, low	t_{WLLK}	$32t_{CYBK}$-5	$32t_{CYBK}$+5	ns	
BICK ↓ to LE delay time	t_{DBKLE}		50	ns	C_L = 50pF
LE period	t_{CYLE}	Typ. = $32t_{CYBK}$		ns	
LE width, high	t_{WHLE}	t_{CYBK}-5	t_{CYBK}+5	ns	
BICK ↓ to R_SH, L_SH delay time	t_{DBKSH}		50	ns	C_L = 50pF
R_SH, L_SH period	t_{CYSH}	Typ. = $64t_{CYBK}$		ns	
R_SH, L_SH width, high	t_{WHSH}	t_{CYBK}-5	t_{CYBK}+5	ns	
BICK ↓ to SDATAI delay time	t_{DBKSD}		50	ns	C_L = 50pF
BICK ↓ to TXP delay time	t_{DBKTX}		50	ns	C_L = 50pF
Control flags					
CLK49, CLK56 ↑ to signals delay time	t_{DBKSG}		15	ns	C_L = 50pF
Signals setup time to CLK49, CLK56 ↑	t_{SKSG}	10		ns	
Signals hold time from CLK49, CLK56 ↑	t_{HKSG}	3		ns	
SYSCLK ↑ to signals delay time	t_{DSKSG}		25	ns	C_L = 50pF
Signals setup time to SYSCLK ↑	t_{SSKSG}	10		ns	
Signals hold time from SYSCLK ↑	t_{HSKSG}	5		ns	
SMPLCLK ↑ to ODVLD delay time	t_{DLKSG}		50	ns	C_L = 50pF
ANLGCTRL setup time to SMPLCLK ↑	t_{SLKSG}	20		ns	
ANLGCTRL hold time from SMPLCLK ↑	t_{HLKSG}	5		ns	
INMODE setup time to R_CLK ↑	t_{SRKSG}	20		ns	
INMODE hold time from R_CLK ↑	t_{HRKSG}	5		ns	
Reset					
Reset* setup time to clocks ↑	t_{SMKRS}	10		ns	
Reset* hold time to clocks ↑	t_{HMKRS}	3		ns	
Reset* width, low	t_{WLRS}	$2t_{CYRK}$+5		ns	

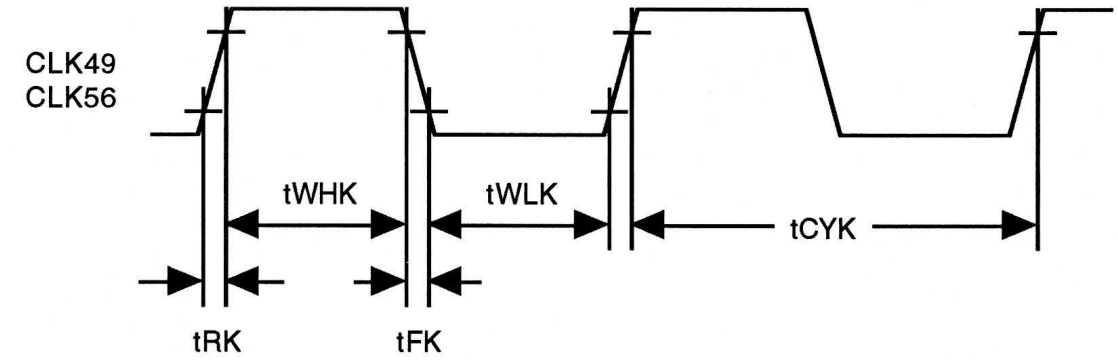
AC Characteristics (continued)

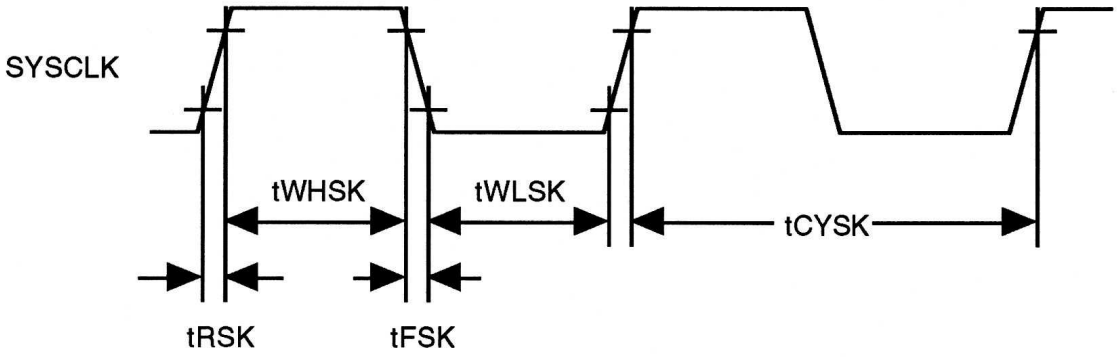
Parameter	Symbol	Min	Max	Unit	Condition
Output enable					
OE* ↓ to signals delay time	t_{DOESG}		50	ns	C_L = 50pF
OE* setup time to SPDIFEN* ↓	t_{SOESE}	0		ns	
OE* hold time from SPDIFEN* ↑	t_{HOESE}	0		ns	
SPDIFEN* ↓ to TXP delay time	t_{DSESG}		50	ns	C_L = 50pF
OE* setup time to DACEN* ↓	t_{SOEDE}	0		ns	
OE* hold time to DACEN* ↑	t_{HOEDE}	0		ns	
DACEN* ↓ to signals delay time	t_{DDESG}		50	ns	C_L = 50pF
System bus read					
A[1:0], BHE*, CS* setup time to RD* ↓	t_{SCSRD}	0		ns	
A[1:0], BHE*, CS* hold time from RD* ↑	t_{HCSRD}	0		ns	
RD* width, low	tWRD	25		ns	
RD* ↓ to D[15:0] delay time	tDDRD		15	ns	C_L = 50pF
D[15:0] hold time from RD* ↑	tHDRD	0	10	ns	
System bus write					
A[1:0], BHE*, CS* setup time to WR* ↓	t_{SCSWR}	0		ns	
A[1:0], BHE*, CS* hold time from WR* ↑	t_{HCSWR}	0		ns	
WR* width, low	tWWR	25		ns	
D[15:0] setup time to WR* ↑	tSDWR		15	ns	
D[15:0] hold time from WR* ↑	tHDWR	0	10	ns	
DMA write					
SYSCLK ↑ to DRQ* ↓ delay time	tDSKDQ		20	ns	C_L = 50pF
DACK* setup time to WR* ↓	t_{SDKWR}	0		ns	
DACK* hold time from WR* ↑	t_{HDKWR}	0		ns	
WR* ↑ to DRQ* ↑ delay time	tDWRDQ		15	ns	C_L = 50pF
IRQ					
SYSCLK ↑ to IRQ* delay time	tDSKIQ		20	ns	C_L = 50pF

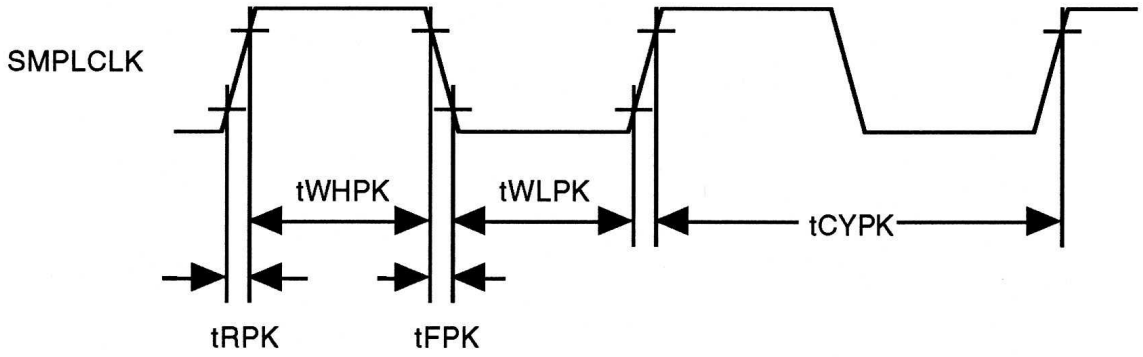
Voltage Thresholds for Timing Measurements

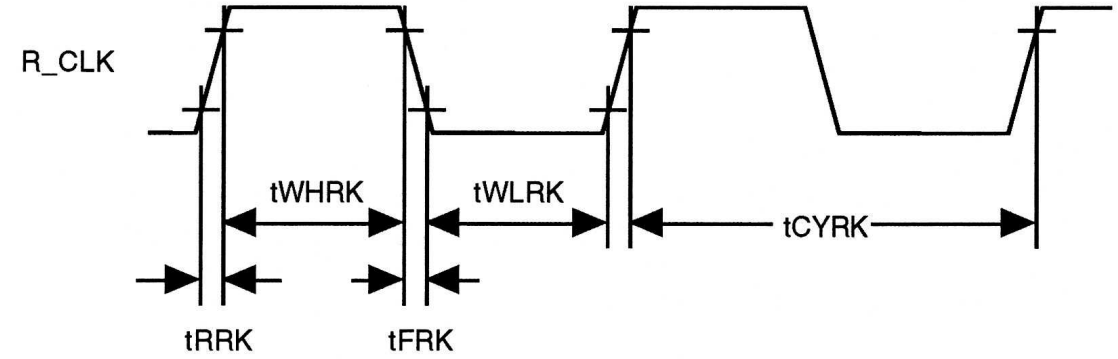


Clock Waveforms

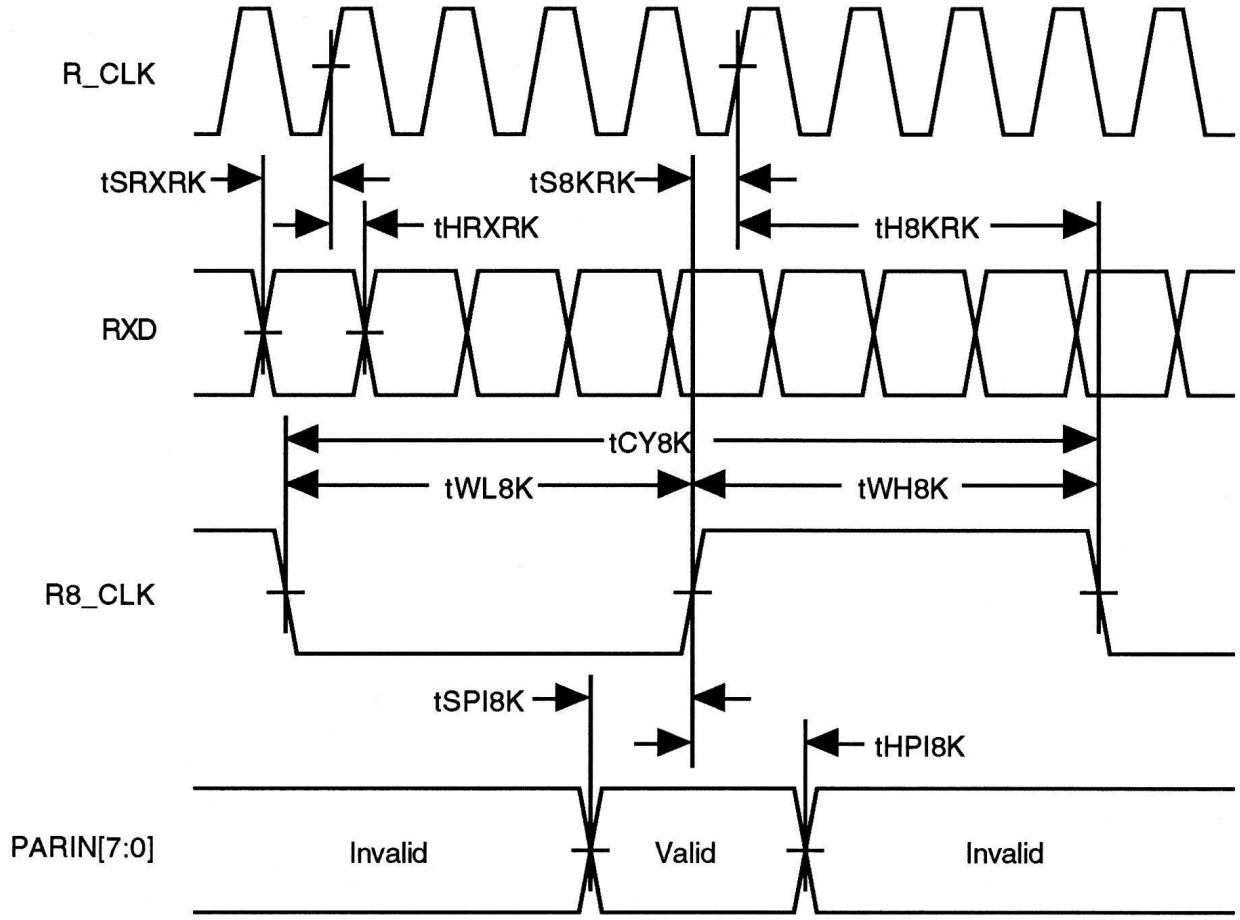




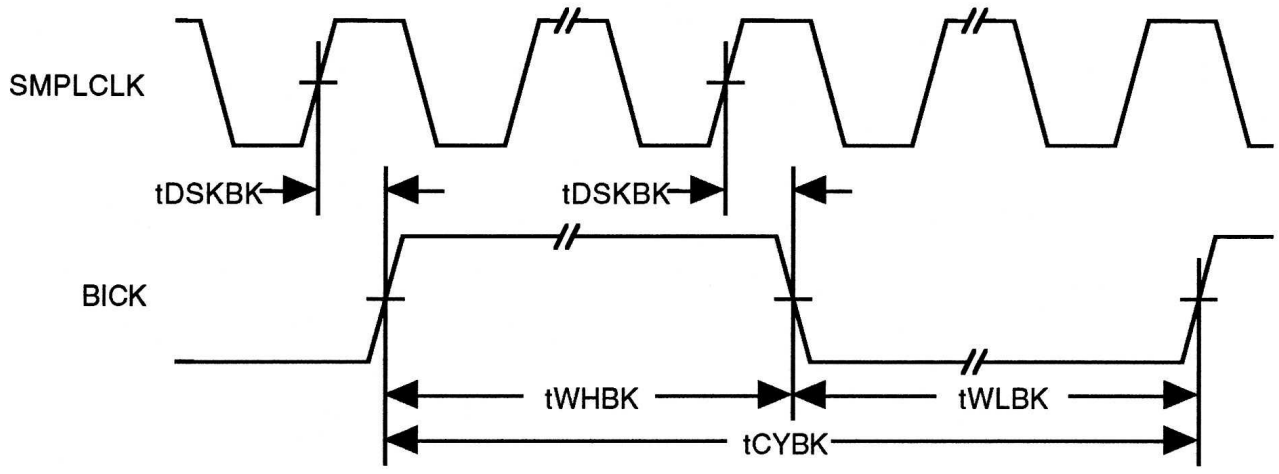




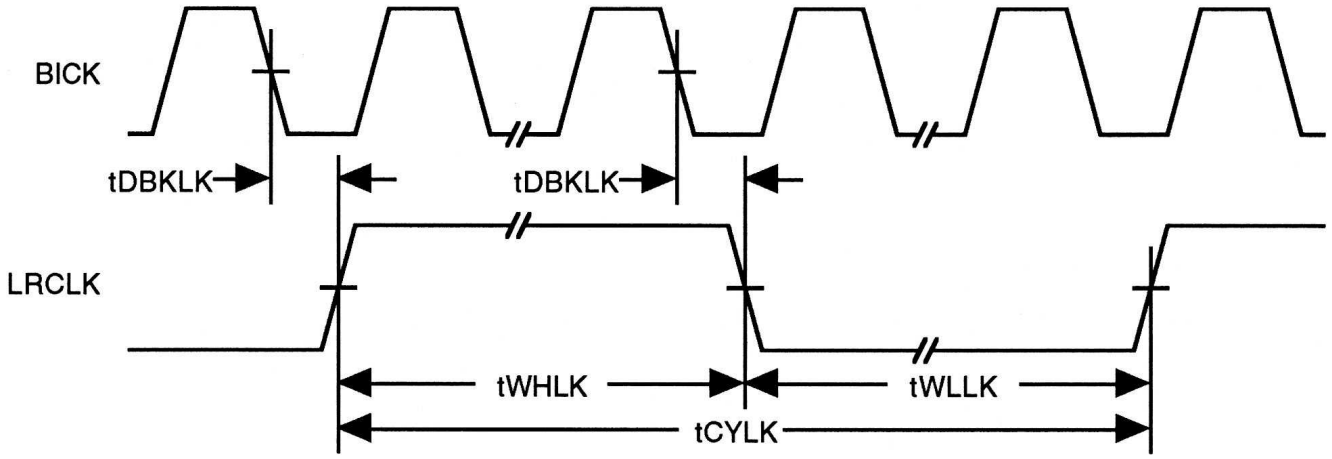
Incoming data



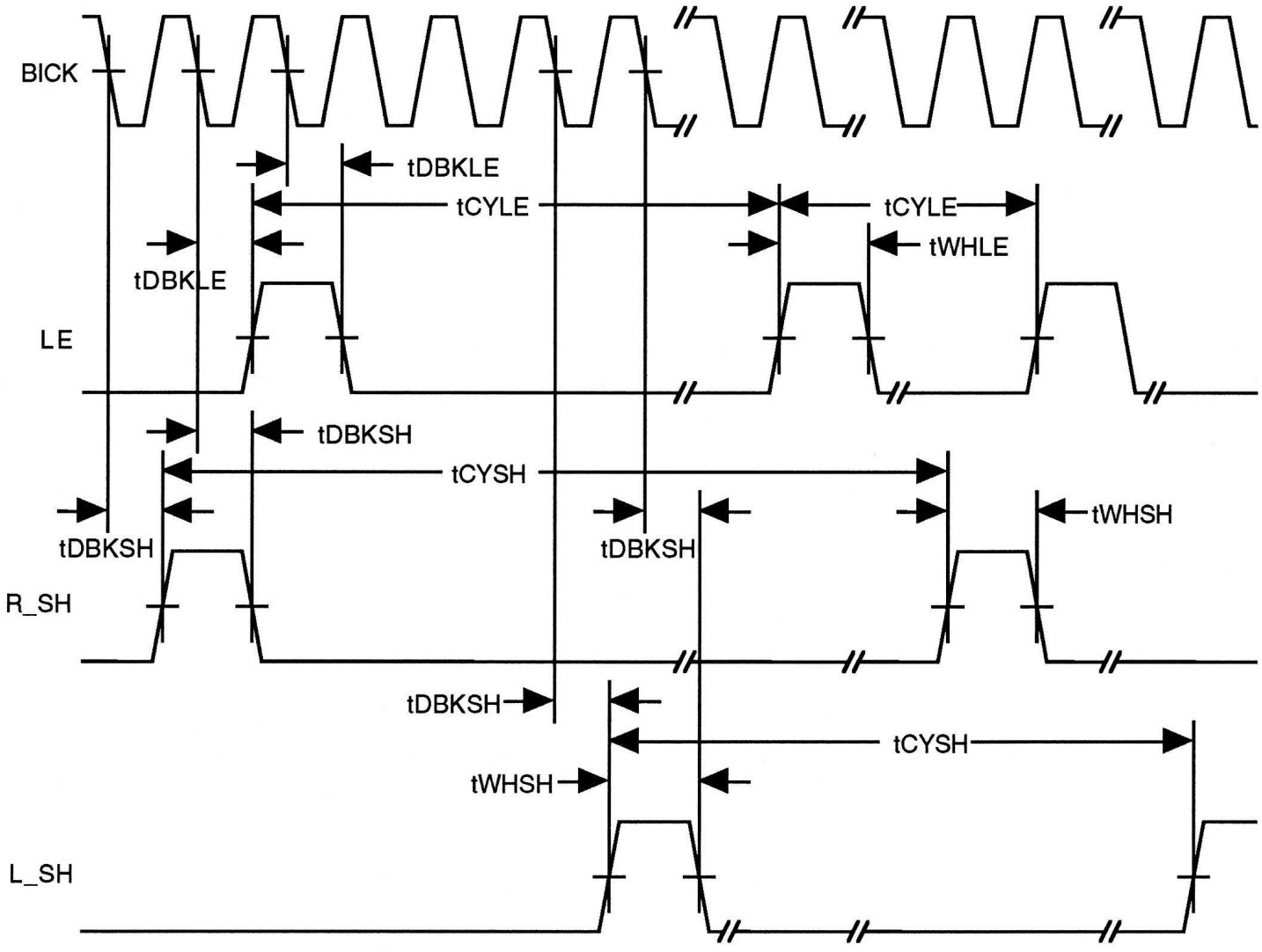
Outgoing data -1



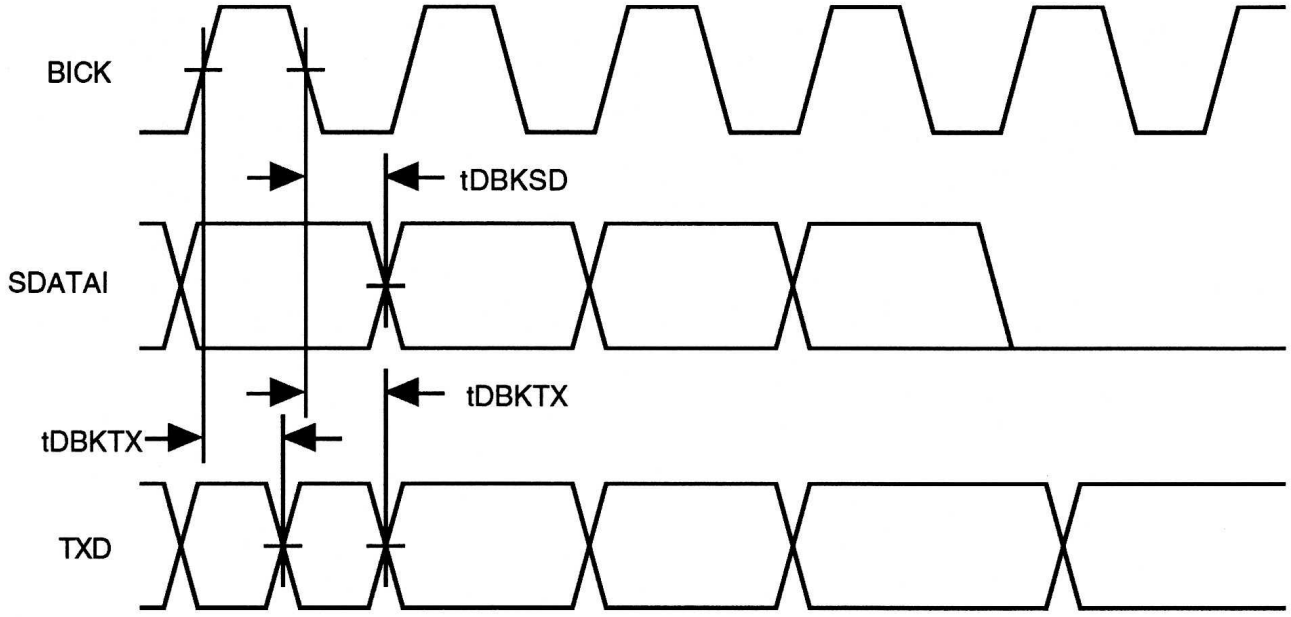
Outgoing data -2



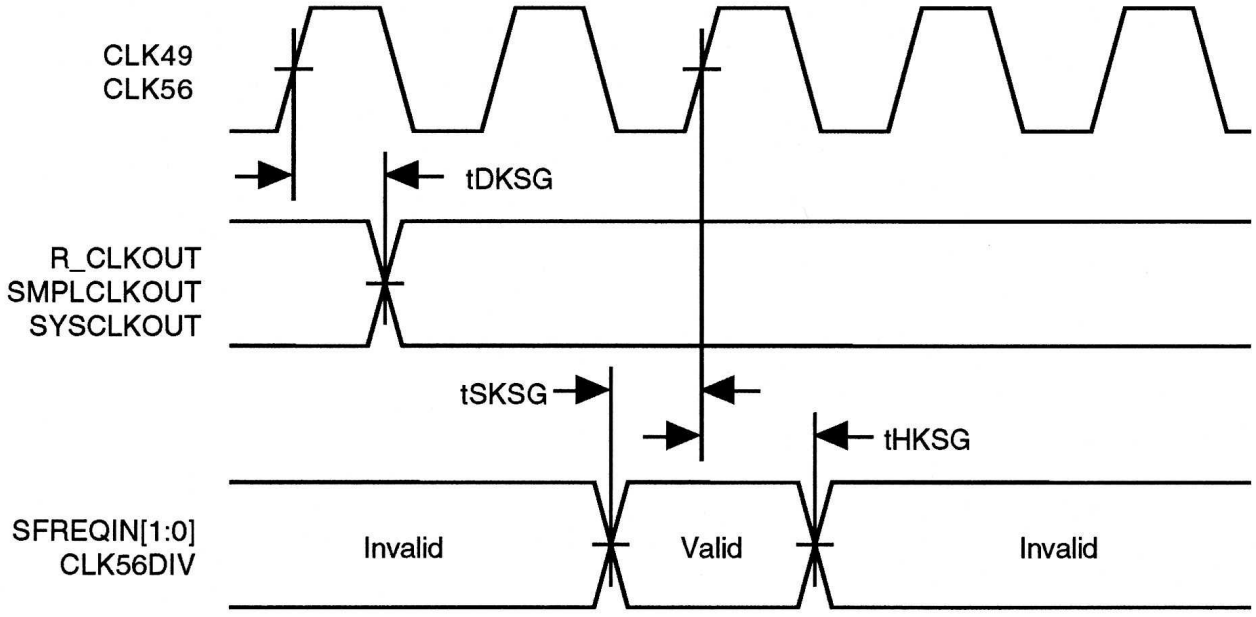
Outgoing data -3



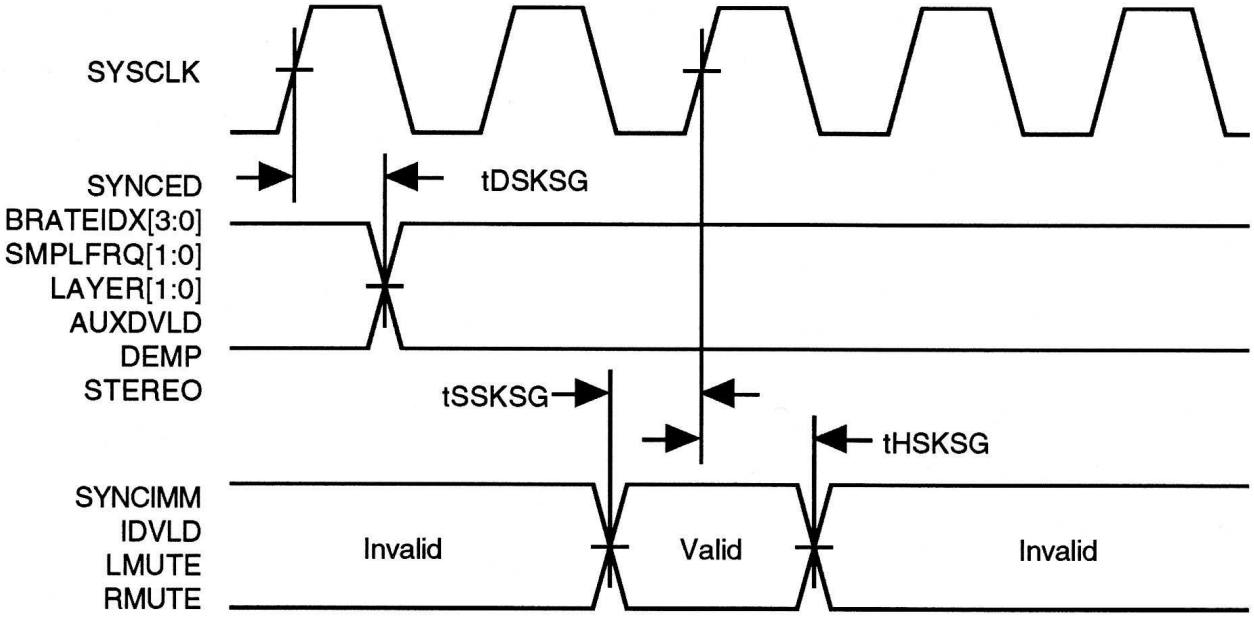
Outgoing data -4



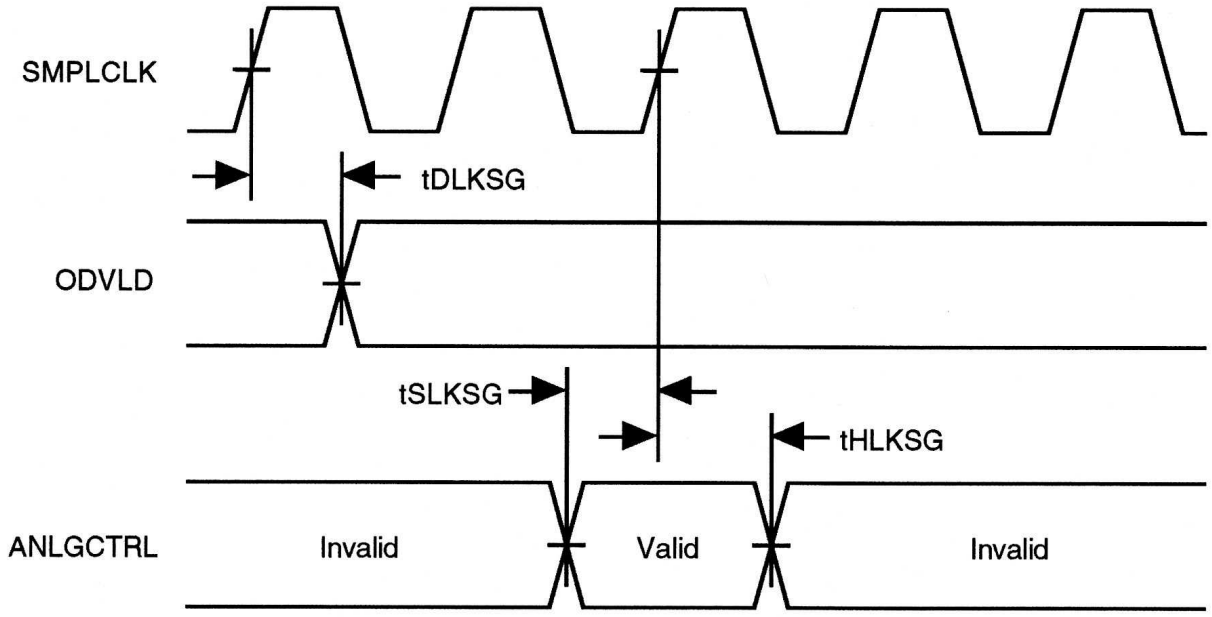
Control flags -1



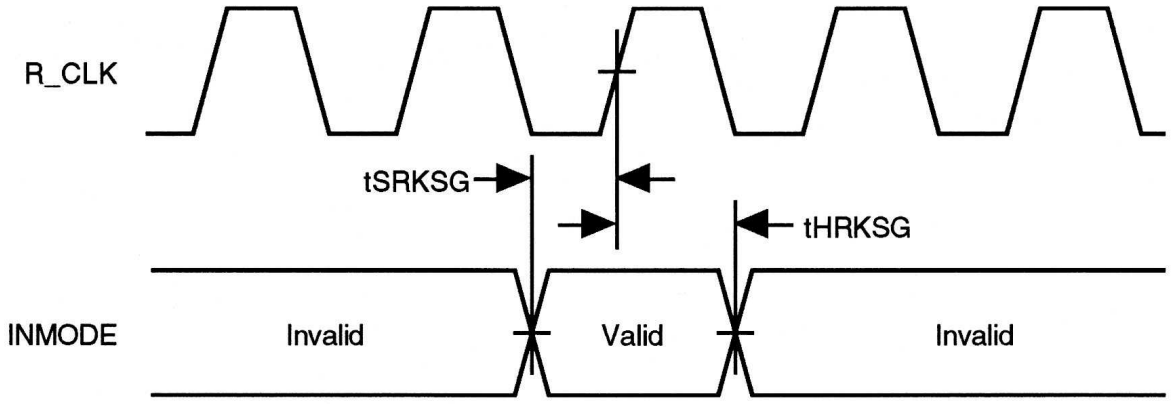
Control flags -2



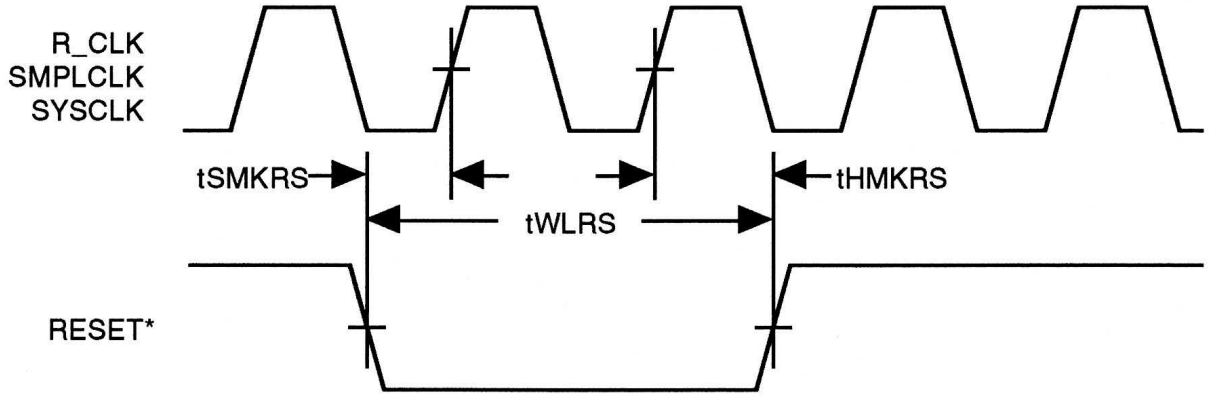
Control flags -3



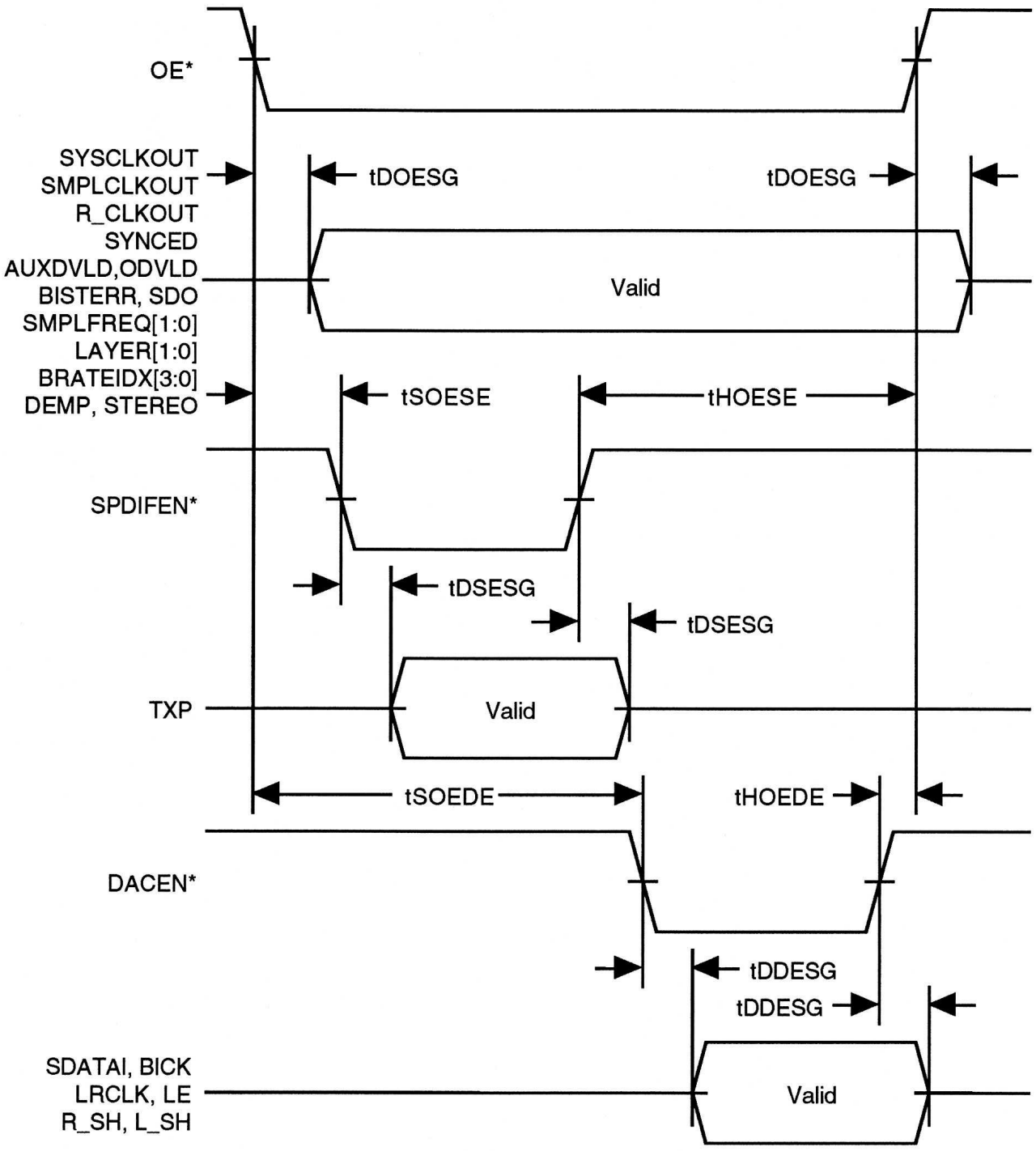
Control flags -4



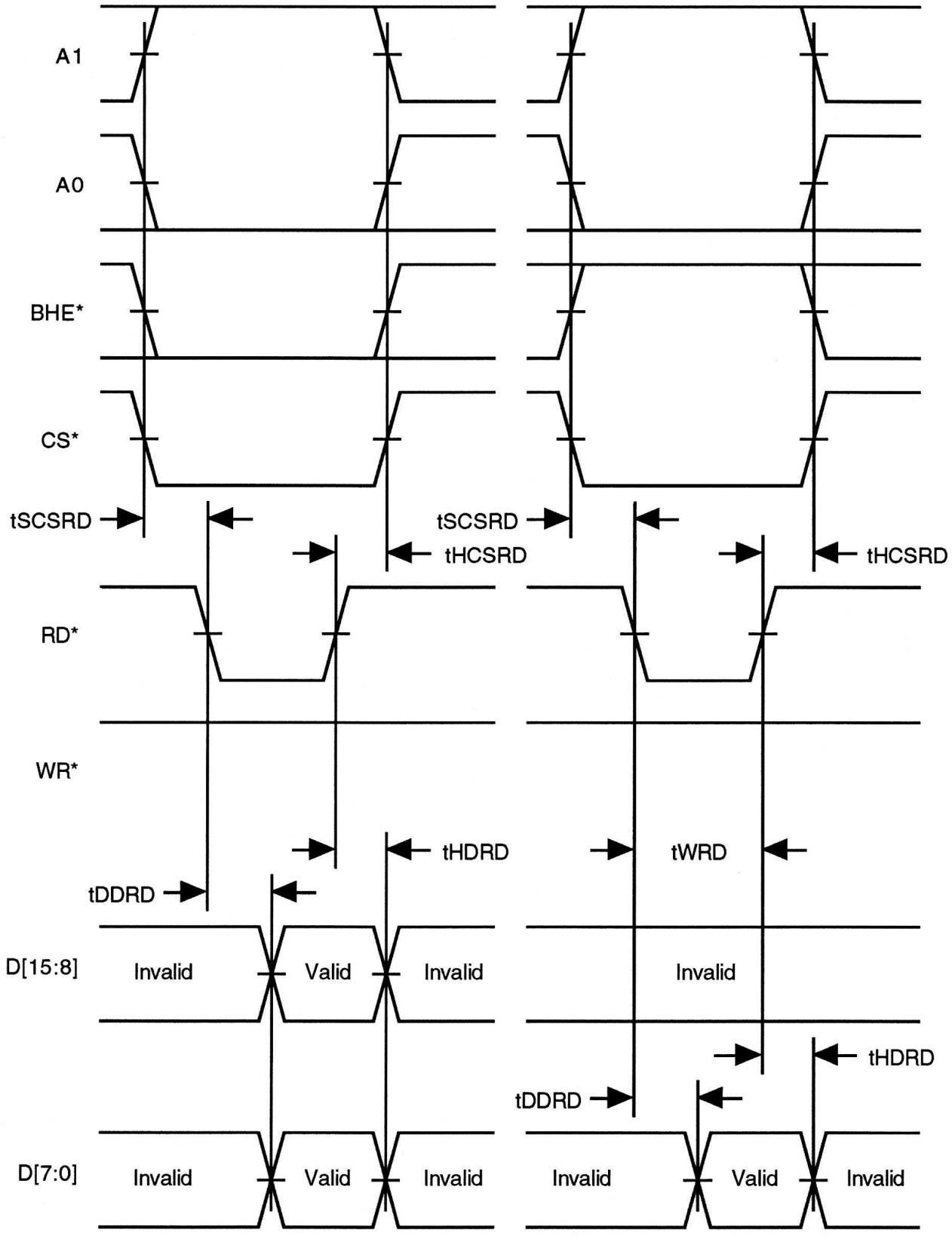
RESET



Output enable



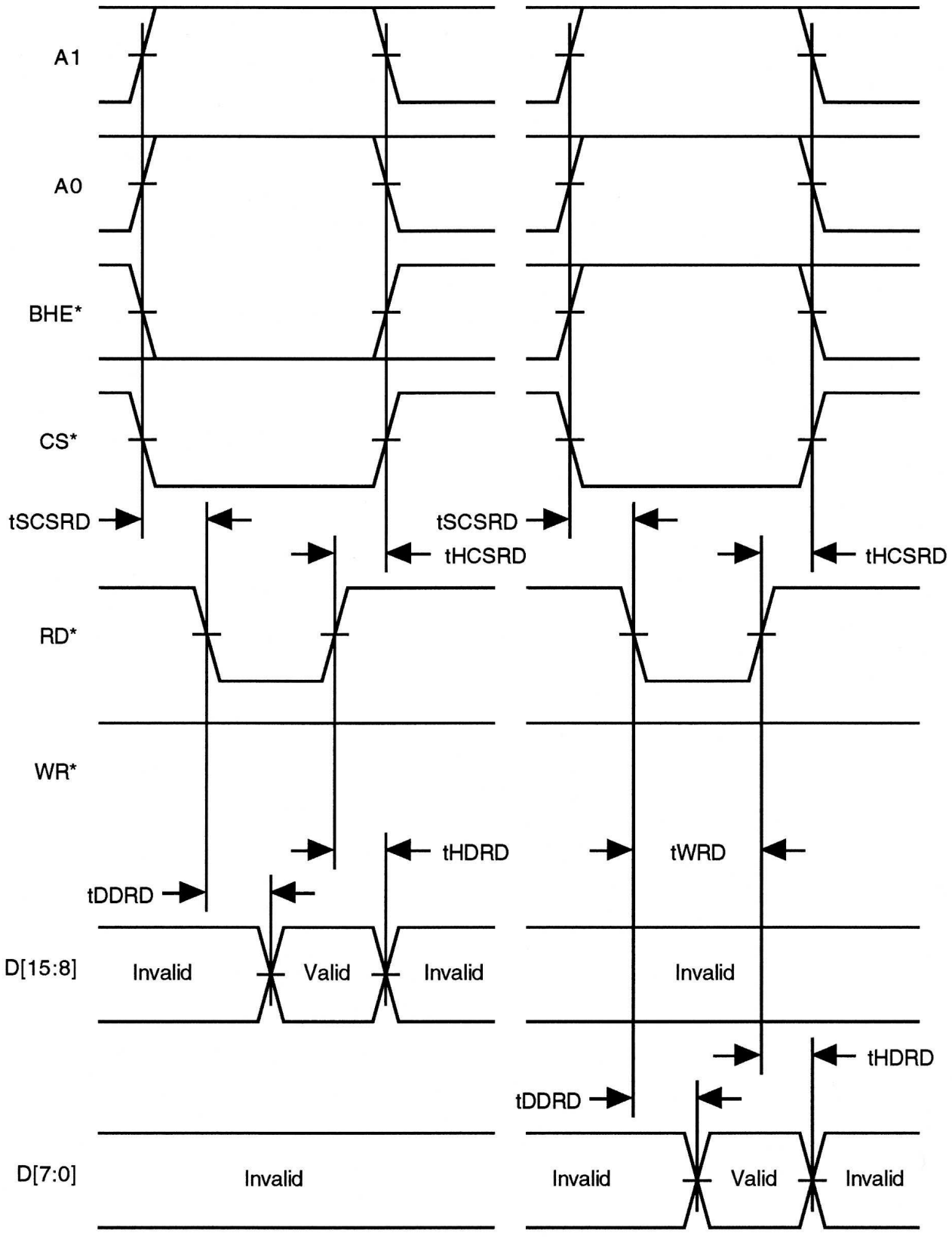
System bus read -1



Even address word

Even address byte

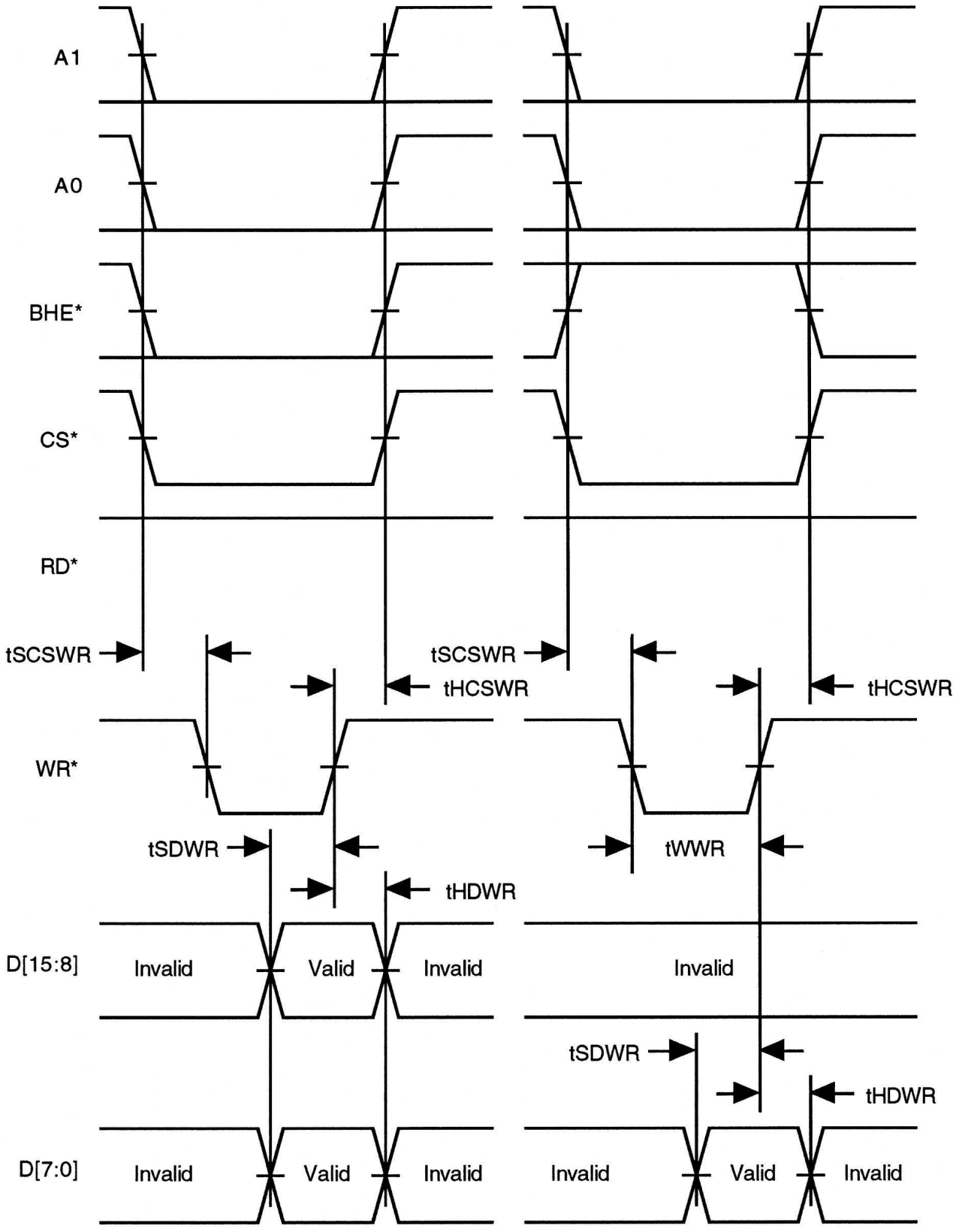
System bus read -2



Odd address byte

Odd address byte

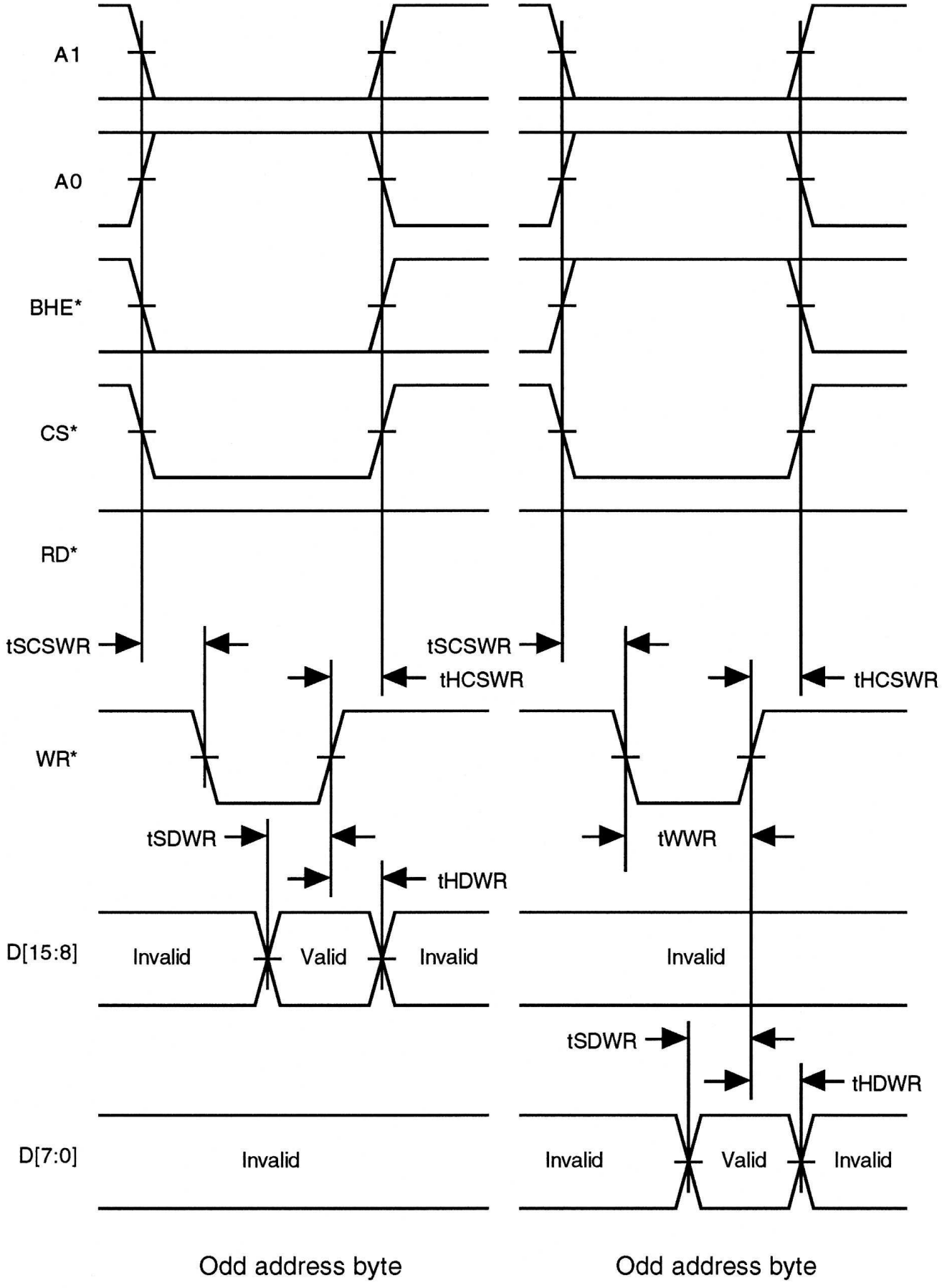
System bus write -1



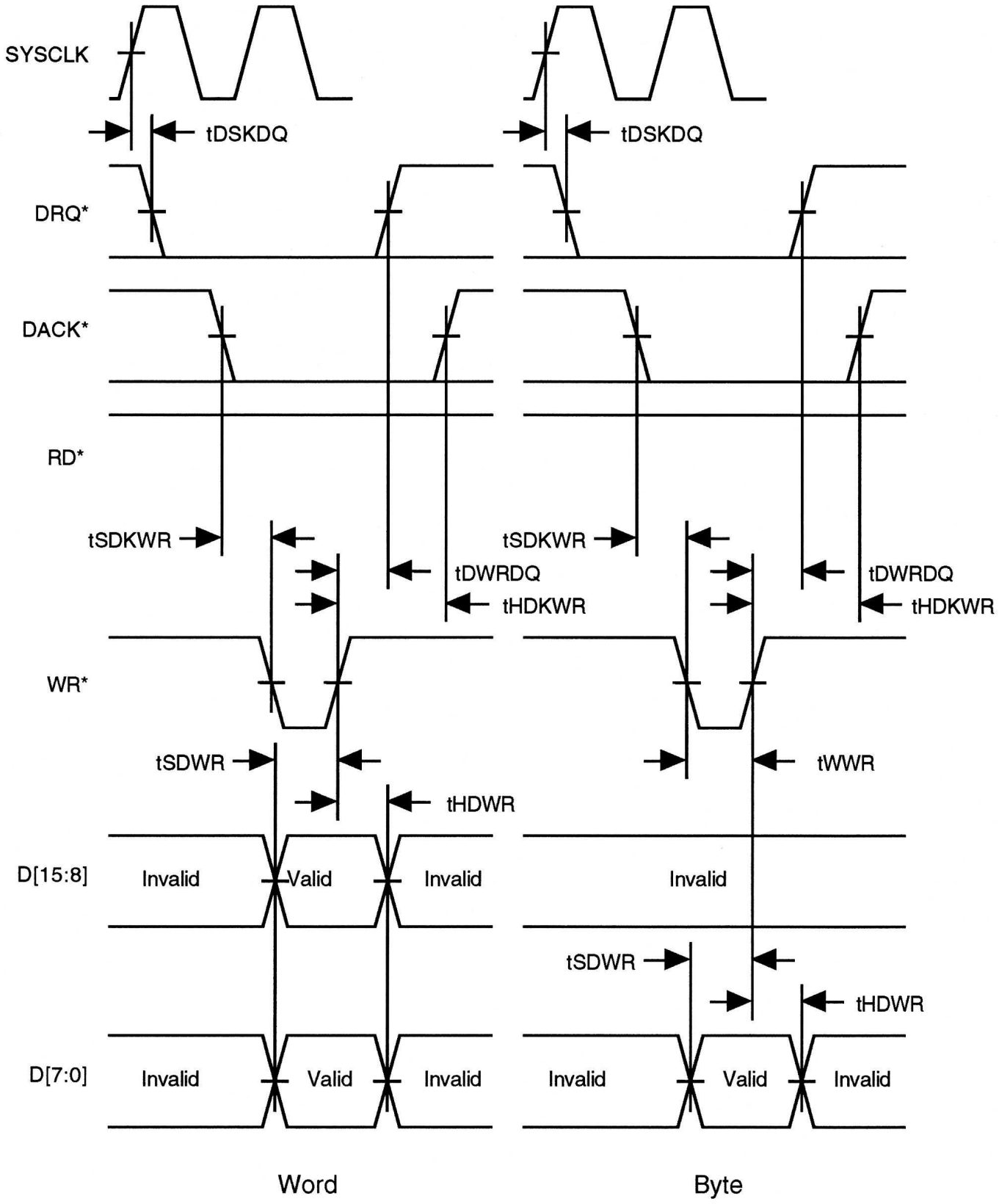
Even address word

Even address byte

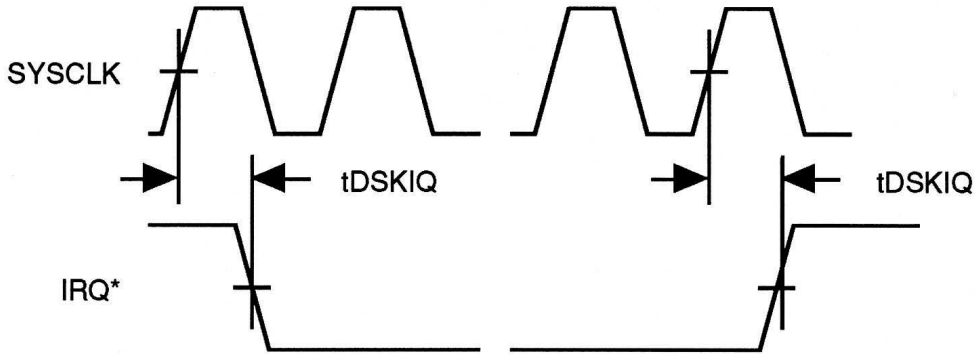
System bus write -2



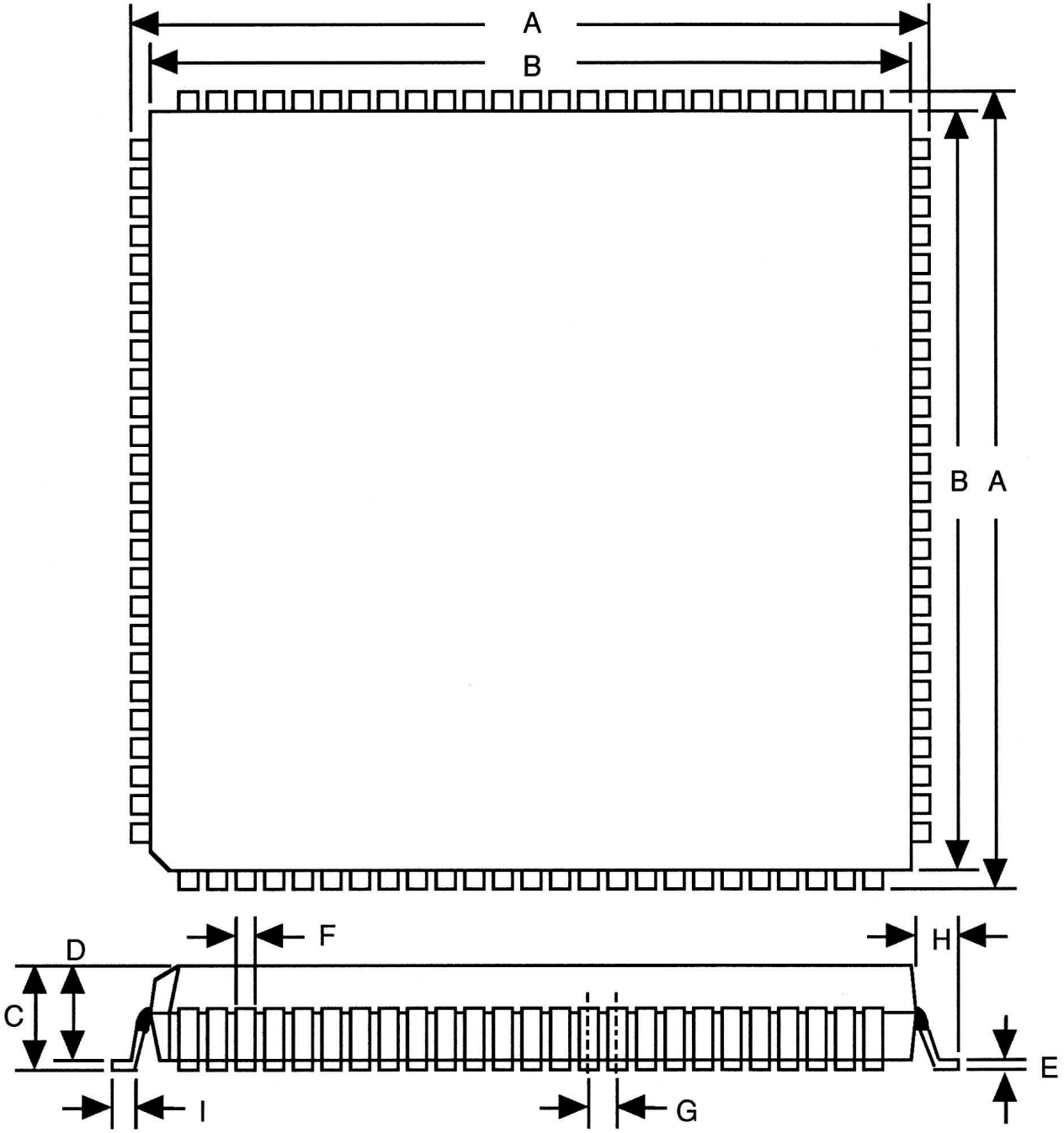
DMA write


SYSCLK
tDSKDQ
DRQ*
DACK*
RD*
tSDKWR
tDWRDQ
tHDKWR
WR*
tSDWR
tHDWR
D[15:8]
Invalid
Valid
Invalid
D[7:0]
Invalid
Valid
Invalid
Word
tSDKWR
tDWRDQ
tHDKWR
tWWR
tSDWR
tHDWR
Invalid
Invalid
Valid
Invalid
Byte

IRQ



Package Drawings



Item	Millimeters	Inches	Item	Millimeters	Inches	Item	Millimeters	Inches
A	16.0±0.3		E	0.12		I	0.5±0.2	
B	14		F	0.20±0.10				
C	<3.05		G	0.5				
D	2.70±0.20		H	1.0				

Application Notes

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The following 2 bits of control register are for test use only. The test function is as follows. (No need to publish this portion)

Symbol	Bit	Register Function (A[1:0]=11)	(default=00000111)
BISTEN*	7	Controls BIST logic.	
		High ; Disables BIST.	Low ; Enables BIST.
TEST	5	Controls test logic.	
		High ; Monitors RXD from IRQ* pin. High ; Inputs BRATEIDX[3:0]. High ; Inputs LAYER[1:0].	Low ; Normal use.