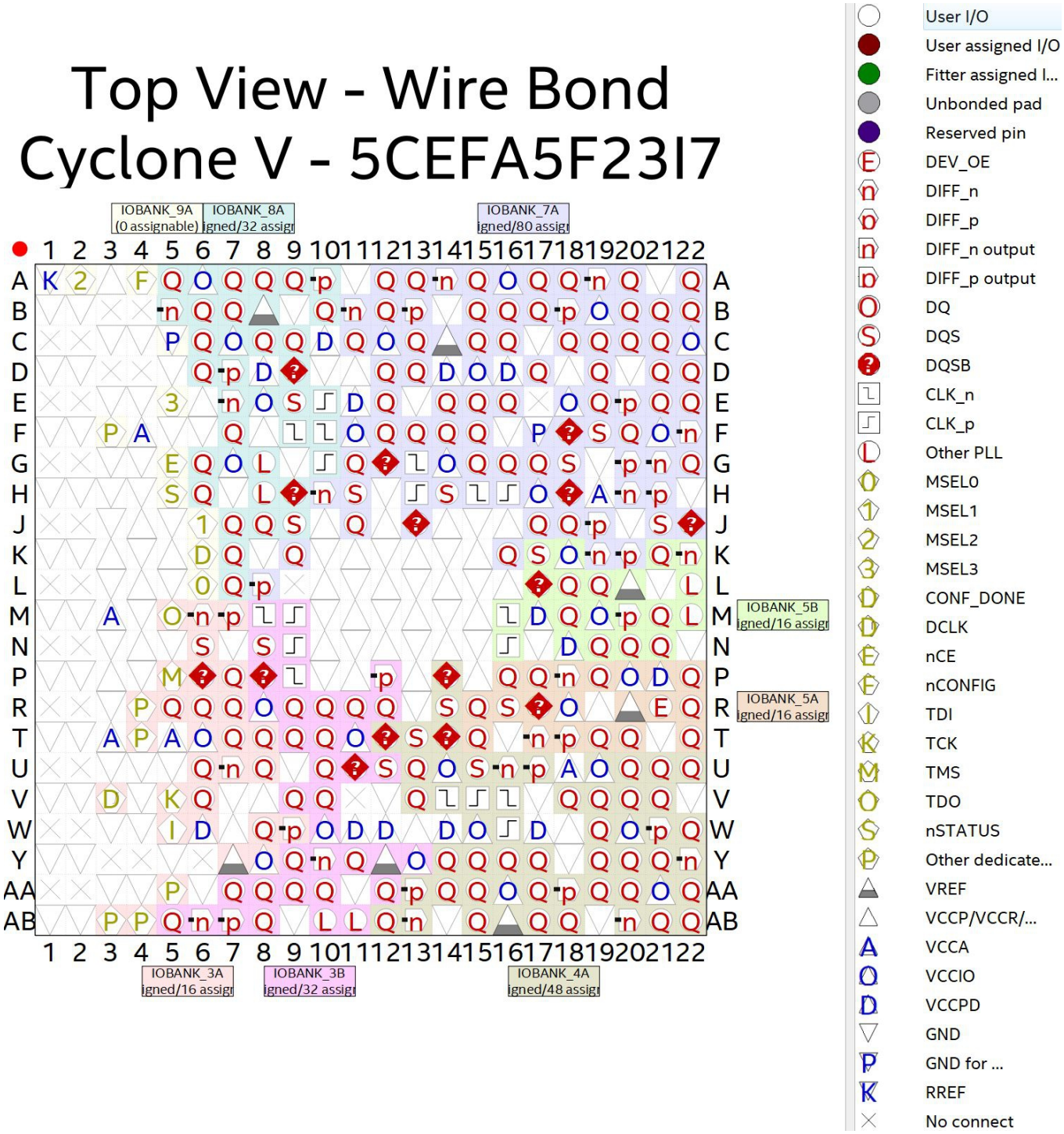
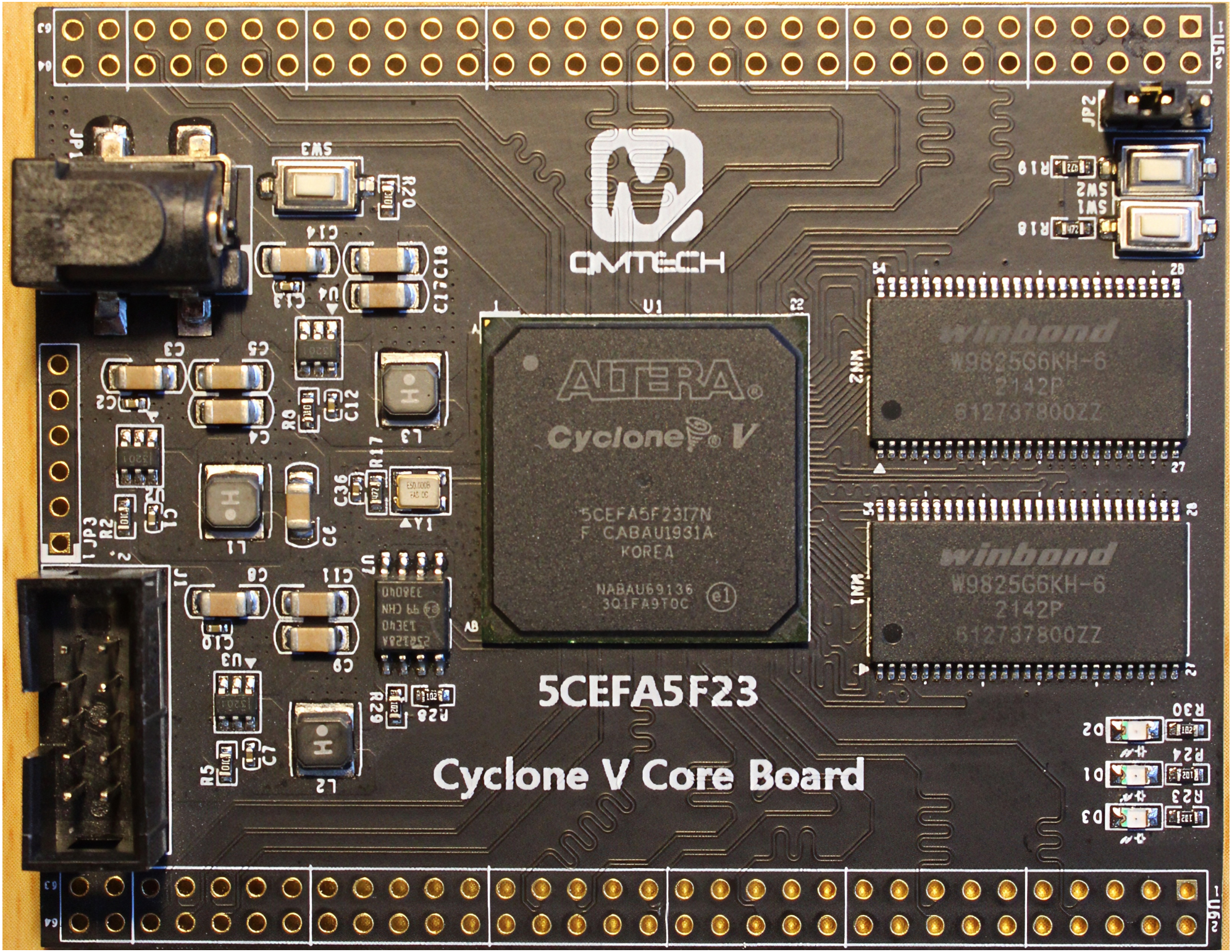
FPGA Board assembled Intel/Altera FPGA "5CEFA5F23I7N"

5C	Cyclone V	- TSMC 28nm low power (28LP) process technology - 1.1V core voltage - 77,000 LEs (Logic Elements) - 29,080 ALMs (Adaptive Logic Modules) - 116,320 Registers, 240 Total I/Os - 240 GP(General Purpose)I/Os - 2 Memory controllers, 4,567,040 Memory bits - 150 DSP(Digital Signal Processor) blocks - 300 18x18 Multipliers - 6 Fractional PLLs (Phase-Locked Loops) - 4 DLLs (Delay-Locked Loops), 16 Global clocks - 60 LVDS (Low Voltage Differential Signal) Transmitters & 60 LVDS Receivers
E	Enhanced logic/memory	
F	No hard PCIe and 2 hard memory controllers	
A5	77k logic elements	
F	Fineline Ball Grid Array (FBGA)	
23	484 pins (22 x 22), 1 mm pitch, 23 mm square	
I	Industrial operating temperature (-40°C to 100°C)	
7	Speed grade	
N	Lead-free packaging	




OMTECH
ALTERA
Cyclone V
5CEFA5F23I7N
F CABAU1931A
KOREA
NABAU69136
3Q1FA9T0C
winbond
W9825G6KH-6
2142P
612737800ZZ
winbond
W9825G6KH-6
2142P
612737800ZZ
5CEFA5F23
Cyclone V Core Board

Example of pin assignment list (hcvcdac.v) for Quartus pin planner

Pin post "U5"						Pin post "U6"					
FPGA Pin	**I/O**	**Pin #**		**I/O**	**FPGA Pin**	**FPGA Pin**	**I/O**	**Pin #**		**I/O**	**FPGA Pin**
GND	-	1	2	-	GND	GND	-	1	2	-	GND
3.3V	-	3	4	-	3.3V	3.3V	-	3	4	-	3.3V
GND	-	5	6	-	GND	GND	-	5	6	-	GND
BANK7A_F19	r[5]	7	8	NC	BANK7A_F18	BANK4A_AB21	NC	7	8	NC	BANK4A_AB20
BANK7A_E19	r[4]	9	10	NC	BANK7A_D19	BANK4A_Y19	NC	9	10	NC	BANK4A_Y20
BANK7A_C20	r[3]	11	12	NC	BANK7A_B20	BANK4A_AA20	NC	11	12	NC	BANK4A_AA19
BANK7A_A20	r[2]	13	14	NC	BANK7A_A19	BANK4A_W19	NC	13	14	NC	BANK4A_V20
BANK7A_C19	r[1]	15	16	NC	BANK7A_C18	BANK4A_AB18	NC	15	16	NC	BANK4A_AB17
BANK7A_A18	r[0]	17	18	NC	BANK7A_A17	BANK4A_U17	NC	17	18	NC	BANK4A_U16
BANK7A_B18	g[5]	19	20	NC	BANK7A_B17	BANK5A_R16	NC	19	20	NC	BANK5A_R17
BANK7A_B16	g[4]	21	22	NC	BANK7A_C16	BANK5A_T15	NC	21	22	NC	BANK5A_R15
BANK7A_C15	g[3]	23	24	NC	BANK7A_B15	BANK4A_R14	NC	23	24	NC	BANK4A_P14
BANK7A_E15	g[2]	25	26	NC	BANK7A_F15	BANK4A_AA15	NC	25	26	NC	BANK4A_AB15
BANK7A_A15	g[1]	27	28	NC	BANK7A_A14	BANK4A_T13	NC	27	28	NC	BANK4A_T12
BANK7A_B13	g[0]	29	30	NC	BANK7A_A13	BANK3B_R11	NC	29	30	NC	BANK3B_R10
BANK7A_B12	b[5]	31	32	NC	BANK7A_A12	BANK4A_AA13	NC	31	32	NC	BANK4A_AA14
BANK7A_G15	b[4]	33	34	NC	BANK7A_F14	BANK4A_Y15	NC	33	34	NC	BANK4A_Y14
BANK7A_H13	b[3]	35	36	NC	BANK7A_G13	BANK4A_AB12	NC	35	36	NC	BANK4A_AB13
BANK7A_D12	b[2]	37	38	NC	BANK7A_E12	BANK3B_AB11	NC	37	38	NC	BANK3B_AB10
BANK7A_H11	b[1]	39	40	NC	BANK7A_G12	BANK3B_V10	NC	39	40	NC	BANK3B_V9
BANK8A_A10	b[0]	41	42	NC	BANK8A_A9	BANK3B_U12	NC	41	42	NC	BANK3B_U11
BANK8A_J9	hsyncn	43	44	NC	BANK8A_H9	BANK3B_R9	NC	43	44	NC	BANK3B_T10
BANK8A_E9	vsyncn	45	46	NC	BANK8A_D9	BANK3A_T8	NC	45	46	NC	BANK3A_T7
BANK8A_H8	NC	47	48	NC	BANK8A_G8	BANK3B_N8	NC	47	48	NC	BANK3B_P8
BANK8A_L7	NC	49	50	NC	BANK8A_K7	BANK3A_M7	NC	49	50	NC	BANK3A_M6
BANK8A_J7	NC	51	52	NC	BANK8A_J8	BANK3A_N6	NC	51	52	NC	BANK3A_P6
BANK8A_A8	NC	53	54	NC	BANK8A_A7	BANK3A_R5	NC	53	54	NC	BANK3A_R6
BANK8A_B6	NC	55	56	NC	BANK8A_B7	BANK3B_AB8	NC	55	56	NC	BANK3B_AA8
BANK8A_C6	NC	57	58	NC	BANK8A_D6	BANK3B_AB7	NC	57	58	NC	BANK3B_AA7
BANK8A_A5	NC	59	60	NC	BANK8A_B5	BANK3B_AB5	NC	59	60	NC	BANK3B_AB6
GND	-	61	62	-	GND	GND	-	61	62	-	GND
VIN (5V)	-	63	64	-	VIN (5V)	VIN (5V)	-	63	64	-	VIN (5V)

QMTECH Cyclone V 5CEFA5F23I7N FPGA Board
(A) Parts assembled
- Altera/Intel Cyclone V 5CEFA5F23I7N 484 pin FBGA (Fineline Ball Grid Array) FPGA
- Winbond W9825GKH-6 32MB (16M x 16) 54 pin 3.3V SDRAM x2 (16M x 32 (A[12:0], D[31:0]) configuration)
- 4 pin 50MHz 3.3V clock oscillator (CLK_50M)
- TI TPS563201 6 pin DC/DC converter IC x3 (VIN (5V) to 3.3V, 2.5V, and 1.1V)
- Micron 3.3V N25Q128A (128Mbit (16M x 8)) 8 pin serial flash memory for SPI boot
  Active Serial Standard Mode (MSEL[4:0] = 10011)
- User push switch x3 (KEY1, KEY2, nCONFIG) (open: 3.3V, push: 0V)
- User 3.3V LED x3 (LED_D1, LED_D2, Power on)

(B) Connectors assembled
- 64 pin 2.54mm pitch header x2 (Total 128 I/O pins) to connect signals between FPGA board and System
- 10 pin JTAG socket for programming FPGA to connect Altera/Intel USB blaster cable
- 5V1A power socket (VIN (5V))

(C) Physical board size (6.7 cm x 8.4 cm)

Altera/Intel USB blaster cable

Altera/Intel Quartus II FPGA Tool
Intel acquired Altera in 2015.
Altera goes back to be an independent company in 2024 and seeks IPO within three years.
Altera focuses on FPGA business and Intel focuses on silicon foundry business. The split must be a good choice.
USA companies are more flexible and resilient compared to Japanese companies.

(1) Verilog HDL Compiler
(2) Logic Synthesizer
(3) IP Handler
(4) Timing Analyzer
(5) Verilog HDL Simulator
ModelSim/QuestaSim by Mentor Graphics acquired by Siemens in 2017. Intel obtained a license from Siemens.
(6) Pin Planner
(7) Netlist Generator
(8) Place & Router
(9) Programmer
(10) On-board Logic Analyzer

I have applied Altera FPGA to my LSI design functional verification on real system twice as below.
- Flash memory controller LSI at ACC Micro in 1997
- USB to flash memory bridge LSI at SanDisk in 2000

Take a look at my actual FPGA application for VGA color bars.

FPGA technology advanced a lot on various fields such as design tools, process technology, packaging technology, and LSI test equipments while all of Japanese semiconductor companies (NEC, Toshiba, Hitachi, etc.) slept for last three decades like a fable of “The Rabbit and The Turtle”. They are “The Rabbits”. “The Lost three decades” is fatal and irreversible. Any fluffy funding efforts must be burnt to the ground like AI projects 1988 scorned.

Pin function assorted by FPGA pin names

FPGA			Board
A1	--	RREF	TL
A2	IOBANK_9A	MSEL2	
A3	--	VCC	2.5V
A4	IOBANK_9A	nCONFIG	
A5	IOBANK_8A	**DQ**	U5-59
A6		VCCIO	3.3V
A7		**DQ**	U5-54
A8			U5-53
A9			U5-42
A10		**DIFF_p O**	U5-41
A11	--	GND	
A12	IOBANK_7A	**DQ**	U5-32
A13			U5-30
A14		**DIFF_n O**	U5-28
A15		**DQ**	U5-27
A16		VCCIO	3.3V
A17		**DQ**	U5-18
A18			U5-17
A19		**DIFF_n O**	U5-14
A20		**DQ**	U5-13
A21	--	GND	
A22	IOBANK_7A	DQ	D30
B1	--	GND	
B2			
B3		NC	DNU1
B4			DNU2
B5	IOBANK_8A	**DIFF_n O**	U5-60
B6		**DQ**	U5-55
B7			U5-56
B8		VREF	GND
B9	--	GND	--
B10	IOBANK_8A	**DQ**	Open
B11	IOBANK_7A	**DIFF_n O**	Open
B12		**DQ**	U5-31
B13		**DIFF_p O**	U5-29
B14	--	GND	--
B15	IOBANK_7A	**DQ**	U5-24
B16			U5-21
B17			U5-20
B18		**DIFF_p O**	U5-19
B19		VCCIO	3.3V
B20		**DQ**	U5-12
B21			D31
B22			D29

FPGA			Board
M1	--	GND	
M2			
M3		VCCA	2.5V PLL6
M4		GND	
M5	IOBANK_3A	TDO	JTAG_TDO
M6		**DIFF_n I**	U6-50
M7		**DIFF_p I**	U6-49
M8	IOBANK_3B	**CLK_n**	Open
M9		**CLK_p**	CLK_50M
M10	--	GND	
M11		VCC	1.1V
M12		GND	
M13		VCC	1.1V
M14		GND	
M15		VCC	1.1V
M16	IOBANK_5B	**CLK_n**	A2
M17		VCCPD	
M18		**DQ**	A0
M19		VCCIO	3.3V
M20		**DIFF_p O**	A1
M21		**DQ**	D8
M22		**PLL**	D9
N1	--	NC	NC19
N2			NC20
N3		GND	
N4		VCC	1.1V
N5		GND	
N6	IOBANK_3A	**DQS**	U6-51
N7	--	GND	--
N8	IOBANK_3B	**DQS**	U6-47
N9		**CLK_p**	Open
N10	--	VCC	1.1V
N11		GND	
N12		VCC	1.1V
N13		GND	
N14		VCC	1.1V
N15		GND	
N16	IOBANK_5B	**CLK_p**	Open
N17	--	GND	
N18	IOBANK_5B	VCCPD	
N19		**DQ**	A10
N20			D14
N21			D15
N22	--	GND	

FPGA			Board
C1	--	NC	NC2
C2			NC1
C3		GND	
C4			
C5	IOBANK_9A	GND for	
C6	IOBANK_8A	**DQ**	U5-57
C7		VCCIO	3.3V
C8		**DQ**	Open
C9			Open
C10	--	VCCPD	3.3V
C11	IOBANK_7A	**DQ**	Open
C12		VCCIO	3.3V
C13		**DQ**	Open
C14		VREF	
C15		**DQ**	U5-23
C16			U5-22
C17	--	GND	
C18	IOBANK_7A	**DQ**	U5-16
C19			U5-15
C20			U5-11
C21			D28
C22		VCCIO	3.3V
D1	--	GND	
D2			
D3		NC	NC13
D4			NC14
D5		GND	
D6	IOBANK_8A	**DQ**	U5-58
D7		**DIFF_p O**	Open
D8	--	VCCPD	3.3V
D9	IOBANK_8A	**DQSB**	U5-46
D10	--	GND	
D11		VCC	2.5V
D12	IOBANK_7A	**DQ**	U5-37 (H16?)
D13			Open
D14	--	VCCPD	3.3V
D15	IOBANK_7A	VCCIO	3.3V
D16	--	VCCPD	3.3V
D17	IOBANK_7A	**DQ**	Open
D18	--	VCC	2.5V
D19	IOBANK_7A	**DQ**	U5-10
D20	--	GND	
D21	IOBANK_7A	**DQ**	D22
D22			D26

FPGA			Board
P1	--	GND	
P2			
P3		VCC	1.1V
P4		GND	
P5	IOBANK_3A	TMS	JTAG_TMS
P6		**DQSB**	U6-52
P7		**DQ**	Open
P8	IOBANK_3B	**DQSB**	
P9		**CLK_n**	
P10	--	GND	
P11		VCC	1.1V
P12	IOBANK_3B	**DIFF_p O**	Open
P13	--	VCC	1.1V
P14	IOBANK_4A	**DQSB**	U6-24
P15	--	VCC	1.1V
P16	IOBANK_5A	**DQ**	RAS
P17			SD_NCS0
P18		**DIFF_n O**	BA1
P19		**DQ**	BA0
P20		VCCIO	3.3V
P21		VCCPD	
P22		**DQ**	D13
R1	--	NC	NC8
R2			NC7
R3		GND	
R4	IOBANK_3A	Other	FPGA_NCSO
R5		**DQ**	U6-53
R6			U6-54
R7			Open
R8	IOBANK_3B	VCCIO	3.3V
R9		**DQ**	U6-43
R10			U6-30
R11			U6-29
R12			Open
R13	--	GND	
R14	IOBANK_4A	**DQS**	U6-23
R15	IOBANK_5A	**DQ**	U6-22
R16		**DQS**	U6-19
R17		**DQSB**	U6-20
R18		VCCIO	3.3V
R19	--	VCC	3.3V
R20	IOBANK_5A	VREF	GND
R21		**DEV_OE**	D11
R22		**DQ**	D12

FPGA			Board
E1	--	NC	NC15
E2			NC16
E3		GND	
E4			
E5	IOBANK_9A	MSEL3	
E6	--	VCC	2.5V
E7	IOBANK_8A	**DIFF_n O**	Open
E8		VCCIO	3.3V
E9		**DQS**	U5-45
E10		**CLK_p**	Open
E11	--	VCCPD	3.3V
E12	IOBANK_7A	**DQ**	U5-38
E13	--	GND	
E14	IOBANK_7A	**DQ**	Open
E15			U5-25
E16			KEY2
E17	--	NC	DNU3
E18	IOBANK_7A	VCCIO	3.3V
E19		**DQ**	U5-9
E20		**DIFF_p O**	D25
E21		**DQ**	DQM3
E22			D24
F1	--	GND	
F2			
F3	IOBANK_9A	Other	
F4	--	VCCA	2.5V PLL2
F5		GND	
F6			
F7	IOBANK_8A	**DQ**	Open
F8	--	VCC	3.3V
F9	IOBANK_8A	**CLK_n**	Open
F10			Open
F11	IOBANK_7A	VCCIO	3.3V
F12		**DQ**	Open
F13			Open
F14			U5-34
F15			U5-26
F16	--	GND	
F17	IOBANK_7A	GND for	GND
F18		**DQSB**	U5-8
F19		**DQS**	U5-7
F20		**DQ**	Open
F21		VCCIO	3.3V
F22		**DIFF_n O**	D23

FPGA			Board
T1	--	GND	
T2			
T3		VCCA	2.5V PLL5
T4	IOBANK_3A	Other	Open
T5	--	VCCA	2.5V PLL1
T6	IOBANK_3A	VCCIO	3.3V
T7		**DQ**	U6-46
T8			U6-45
T9	IOBANK_3B		Open
T10			U6-44
T11		VCCIO	3.3V
T12	IOBANK_4A	**DQSB**	U6-28
T13		**DQS**	U6-27
T14		**DQSB**	Open
T15	IOBANK_5A	**DQ**	U6-21
T16	--	GND	
T17	IOBANK_5A	**DIFF_n I**	Open
T18		**DIFF_p I**	Open
T19		**DQ**	CAS
T20			LED_D2
T21	--	GND	
T22	IOBANK_5A	**DQ**	D10
U1	--	NC	NC21
U2			NC22
U3		GND	
U4			
U5			
U6	IOBANK_3A	**DQ**	Open
U7		**DIFF_n O**	Open
U8		**DQ**	Open
U9	--	GND	
U10	IOBANK_3B	**DQ**	Open
U11		**DQSB**	U6-42
U12		**DQS**	U6-41
U13	IOBANK_4A	**DQ**	Open
U14		VCCIO	3.3V
U15		**DQS**	Open
U16		**DIFF_n I**	U6-18
U17		**DIFF_p I**	U6-17
U18	--	VCCA	2.5V PLL3
U19	IOBANK_4A	VCCIO	3.3V
U20		**DQ**	SDWE
U21			DQM0
U22			D7

FPGA			Board
G1	--	NC	NC4
G2			NC3
G3		GND	
G4			
G5	IOBANK_9A	nCE	
G6	IOBANK_8A	**DQ**	Open
G7		VCCIO	3.3V
G8		**PLL**	U5-48
G9	--	GND	
G10	IOBANK_8A	**CLK_p**	Open
G11	IOBANK_7A	**DQ**	Open
G12		**DQSB**	U5-40
G13		**CLK_n**	U5-36
G14		VCCIO	3.3V
G15		**DQ**	U5-33
G16			Open
G17			SDCKE0
G18		**DQS**	SDCLK0
G19	--	GND	
G20	IOBANK_7A	**DIFF_p I**	Open
G21		**DIFF_n I**	D27
G22		**DQ**	D21
H1	--	GND	
H2			
H3			
H4			
H5	IOBANK_9A	nSTATUS	
H6	IOBANK_8A	**DQ**	Open
H7	--	GND	
H8	IOBANK_8A	**PLL**	U5-47
H9		**DQSB**	U5-44
H10	IOBANK_7A	**DIFF_n O**	Open
H11		**DQS**	U5-39
H12	--	GND	
H13	IOBANK_7A	**CLK_p**	U5-35
H14		**DQS**	Open
H15		**CLK_n**	Open
H16		**CLK_p**	(H16?)
H17		VCCIO	3.3V
H18		**DQSB**	A11
H19	--	VCCA	2.5V PLL4
H20	IOBANK_7A	**DIFF_n I**	A12
H21		**DIFF_p I**	D20
H22	--	GND	

FPGA			Board
V1	--	GND	
V2			
V3	IOBANK_3A	DCLK	FPGA_DCLK
V4	--	GND	
V5	IOBANK_3A	TCLK	JTAG_TCK
V6		**DQ**	Open
V7	--	GND	
V8		VCC	3.3V
V9	IOBANK_3B	**DQ**	U6-40
V10			U6-39
V11	--	NC	NC26
V12		GND	
V13	IOBANK_4A	**DQ**	Open
V14		**CLK_n**	Open
V15		**CLK_p**	Open
V16		**CLK_n**	Open
V17	--	GND	
V18	IOBANK_4A	**DQ**	Open
V19			LED_D1
V20			U6-14
V21			D6
V22	--	GND	
W1	--	NC	NC10
W2			NC9
W3		GND	
W4			
W5	IOBANK_3A	TDI	JTAG_TDI
W6		VCCPD	3.3V
W7	--	VCC	2.5V
W8	IOBANK_3A	**DQ**	Open
W9		**DIFF_p O**	Open
W10	IOBANK_3B	VCCIO	3.3V
W11	--	VCCPD	3.3V
W12			3.3V
W13		VCC	2.5V
W14		VCCPD	3.3V
W15	IOBANK_4A	VCCIO	3.3V
W16		**CLK_p**	Open
W17	--	VCCPD	3.3V
W18		VCC	2.5V
W19	IOBANK_4A	**DQ**	U6-13
W20		VCCIO	3.3V
W21		**DIFF_p O**	D5
W22		**DQ**	D4

FPGA			Board
J1	--	NC	NC17
J2			NC18
J3		GND	
J4		VCC	1.1V
J5		GND	
J6	IOBANK_9A	MSEL1	
J7	IOBANK_8A	**DQ**	U5-51
J8			U5-52
J9		**DQS**	U5-43
J10	--	VCC	1.1V
J11	IOBANK_7A	**DQ**	Open
J12	--	VCC	1.1V
J13	IOBANK_7A	**DQSB**	Open
J14	--	VCC	1.1V
J15		GND	
J16		VCC	1.1V
J17	IOBANK_7A	**DQ**	KEY1
J18			A8
J19		**DIFF_p O**	A9
J20	--	GND	
J21	IOBANK_7A	**DQS**	D19
J22		**DQSB**	D18
K1	--	GND	
K2			
K3		VCC	1.1V
K4		GND	
K5		VCC	1.1V
K6	IOBANK_9A	CONF_DONE	
K7	IOBANK_8A	**DQ**	U5-50
K8	--	GND	
K9	IOBANK_7A	**DQ**	Open
K10	--	GND	
K11		VCC	1.1V
K12		GND	
K13		VCC	1.1V
K14		GND	
K15		VCC	1.1V
K16	IOBANK_7A	**DQ**	A6
K17	IOBANK_5B	**DQS**	A7
K18		VCCIO	3.3V
K19	IOBANK_7A	**DIFF_n I**	Open
K20		**DIFF_p I**	DQM2
K21	IOBANK_5B	**DQ**	D17
K22		**DIFF_n O**	D16

FPGA			Board
Y1	--	GND	
Y2			
Y3		NC	NC23
Y4			NC24
Y5		GND	
Y6		NC	NC25
Y7	IOBANK_3A	VREF	GND
Y8		VCCIO	3.3V
Y9	IOBANK_3B	**DQ**	Open
Y10		**DIFF_n O**	Open
Y11		**DQ**	Open
Y12		VREF	GND
Y13		VCCIO	3.3V
Y14	IOBANK_4A	**DQ**	U6-34
Y15			U6-33
Y16			Open
Y17			Open
Y18	--	GND	
Y19	IOBANK_4A	**DQ**	U6-9
Y20			U6-10
Y21			D3
Y22		**DIFF_n O**	D2
AA1	--	NC	NC12
AA2			NC11
AA3		GND	
AA4			
AA5	IOBANK_3A	Other	Open
AA6	--	GND	
AA7	IOBANK_3B	**DQ**	U6-58
AA8			U6-56
AA9			Open
AA10			Open
AA11	--	GND	Open
AA12	IOBANK_3B	**DQ**	
AA13	IOBANK_4A	**DIFF_p O**	U6-31
AA14		**DQ**	U6-32
AA15			U6-25
AA16		VCCIO	3.3V
AA17		**DQ**	Open
AA18		**DIFF_p O**	Open
AA19		**DQ**	U6-12
AA20			U6-11
AA21		VCCIO	3.3V
AA22		**DQ**	D0

FPGA			Board
L1	--	NC	NC6
L2			NC5
L3		GND	
L4		VCC	1.1V
L5		GND	
L6	IOBANK_9A	MSEL0	
L7	IOBANK_8A	**DQ**	U5-49
L8	IOBANK_7A	**DIFF_p O**	Open
L9	--	NC	DNU4
L10		VCC	1.1V
L11		GND	
L12		VCC	1.1V
L13		GND	
L14		VCC	1.1V
L15		GND	
L16		VCC	1.1V
L17	IOBANK_5B	**DQSB**	A3
L18		**DQ**	A5
L19			A4
L20		VREF	GND
L21	--	GND	
L22	IOBANK_5B	**PLL**	DQM1

FPGA			Board
AB1	--	GND	
AB2			
AB3	IOBANK_3A	Other	FPGA_DATA1
AB4			FPGA_ADSO
AB5	IOBANK_3B	**DQ**	U6-59
AB6		**DIFF_n O**	U6-60
AB7		**DIFF_p O**	U6-57
AB8		**DQ**	U6-55
AB9	--	GND	
AB10	IOBANK_3B	**PLL**	U6-38
AB11			U6-37
AB12	IOBANK_4A	**DQ**	U6-35
AB13		**DIFF_n O**	U6-36
AB14	--	GND	
AB15	IOBANK_4A	**DQ**	U6-26
AB16		VREF	GND
AB17		**DQ**	U6-16
AB18			U6-15
AB19	--	GND	
AB20	IOBANK_4A	**DIFF_n O**	U6-8
AB21		**DQ**	U6-7
AB22			D1

Pin function assorted by FPGA IOBANKs

FPGA			Board
IOBANK_3A	M5	TDO	JTAG_TDO
	M6	**DIFF_n I**	U6-50
	M7	**DIFF_p I**	U6-49
	N6	**DQS**	U6-51
	P5	TMS	JTAG_TMS
	P6	**DQSB**	U6-52
	P7	**DQ**	Open
	R4	Other	FPGA_NCSO
	R5	**DQ**	U6-53
	R6		U6-54
	R7		Open
	T4	Other	Open
	T5	VCCA	
	T6	VCCIO	3.3V
	T7	**DQ**	U6-46
	T8		U6-45
	U6	**DQ**	Open
	U7	**DIFF_n O**	Open
	U8	**DQ**	Open
	V3	DCLK	FPGA_DCLK
	V5	TCLK	JTAG_TCK
	V6	**DQ**	Open
	W5	TDI	JTAG_TDI
	W6	VCCPD	
	W8	**DQ**	Open
	W9	**DIFF_p O**	Open
	Y7	VREF	GND
	Y8	VCCIO	3.3V
	AA5	Other	Open
	AB3		FPGA_DATA1
	AB4		FPGA_ADSO
		16 I/Os	In I/O Out

FPGA			Board
IOBANK_3B	M8	**CLK_n**	Open
	M9	**CLK_p**	CLK_50M
	N8	**DQS**	U6-47
	N9	**CLK_p**	Open
	P8	**DQSB**	U6-48
	P9	**CLK_n**	Open
	P12	**DIFF_p O**	Open
	R8	VCCIO	3.3V
	R9	**DQ**	U6-43
	R10		U6-30
	R11		U6-29
	R12		Open
	T9	**DQ**	Open
	T10		U6-44
	T11	VCCIO	3.3V
	U10	**DQ**	Open
	U11	**DQSB**	U6-42
	U12	**DQS**	U6-41
	V9	**DQ**	U6-40
	V10		U6-39
	W10	VCCIO	3.3V
	Y9	**DQ**	Open
	Y10	**DIFF_n O**	Open
	Y11	**DQ**	Open
	Y12	VREF	GND
	Y13	VCCIO	3.3V
	AA7	**DQ**	U6-58
	AA8		U6-56
	AA9		Open
	AA10		Open
	AA12		Open
	AB5	**DQ**	U6-59
	AB6	**DIFF_n O**	U6-60
	AB7	**DIFF_p O**	U6-57
	AB8	**DQ**	U6-55
	AB10	**PLL**	U6-38
	AB11		U6-37
		32 I/Os	In I/O Out

FPGA			Board
IOBANK_4A	P14	**DQSB**	U6-24
	R14	**DQS**	U6-23
	T12	**DQSB**	U6-28
	T13	**DQS**	U6-27
	T14	**DQSB**	Open
	U13	**DQ**	Open
	U14	VCCIO	3.3V
	U15	**DQS**	Open
	U16	**DIFF_n I**	U6-18
	U17	**DIFF_p I**	U6-17
	U19	VCCIO	3.3V
	U20	**DQ**	SDWE
	U21		DQM0
	U22		D7
	V13	**DQ**	Open
	V14	**CLK_n**	Open
	V15	**CLK_p**	Open
	V16	**CLK_n**	Open
	V18	**DQ**	Open
	V19		LED_D1
	V20		U6-14
	V21		D6
	W15	VCCIO	3.3V
	W16	**CLK_p**	Open
	W19	**DQ**	U6-13
	W20	VCCIO	3.3V
	W21	**DIFF_p O**	D5
	W22	**DQ**	D4
	Y14		U6-34
	Y15		U6-33
	Y16		Open
	Y17		Open
	Y19		U6-9
	Y20		U6-10
	Y21		D3
	Y22	**DIFF_n O**	D2

FPGA			Board
IOBANK_4A	AA13	**DIFF_p O**	U6-31
	AA14	**DQ**	U6-32
	AA15		U6-25
	AA16	VCCIO	3.3V
	AA17	**DQ**	Open
	AA18	**DIFF_p O**	Open
	AA19	**DQ**	U6-12
	AA20		U6-11
	AA21	VCCIO	3.3V
	AA22	**DQ**	D0
	AB12		U6-35
	AB13	**DIFF_n O**	U6-36
	AB15	**DQ**	U6-26
	AB16	VREF	GND
	AB17	**DQ**	U6-16
	AB18		U6-15
	AB20	**DIFF_n O**	U6-8
	AB21	**DQ**	U6-7
	AB22		D1
		48 I/Os	In I/O Out

FPGA			Board
IOBANK_5A	P16	**DQ**	RAS
	P17		SD_NCS0
	P18	**DIFF_n O**	BA1
	P19	**DQ**	BA0
	P20	VCCIO	3.3V
	P21	VCCPD	
	P22	**DQ**	D13
	R15		U6-22
	R16	**DQS**	U6-19
	R17	**DQSB**	U6-20
	R18	VCCIO	3.3V
	R20	VREF	GND
	R21	**DEV_OE**	D11
	R22	**DQ**	D12
	T15		U6-21
	T17	**DIFF_n I**	Open
	T18	**DIFF_p I**	Open
	T19	**DQ**	CAS
	T20		LED_D2
	T22		D10
		16 I/Os	In I/O Out

FPGA			Board
IOBANK_5B	K17	**DQS**	A7
	K18	VCCIO	3.3V
	K21	**DQ**	D17
	K22	**DIFF_n O**	D16
	L17	**DQSB**	A3
	L18	**DQ**	A5
	L19		A4
	L20	VREF	GND
	L22	**PLL**	DQM1
	M16	**CLK_n**	A2
	M17	VCCPD	
	M18	**DQ**	A0
	M19	VCCIO	3.3V
	M20	**DIFF_p O**	A1
	M21	**DQ**	D8
	M22	**PLL**	D9
	N16	**CLK_p**	Open
	N18	VCCPD	
	N19	**DQ**	A10
	N20		D14
	N21		D15
		16 I/Os	In I/O Out

FPGA			Board
IOBANK_7A	A12	**DQ**	U5-32
	A13		U5-30
	A14	**DIFF_n O**	U5-28
	A15	**DQ**	U5-27
	A16	VCCIO	3.3V
	A17	**DQ**	U5-18
	A18		U5-17
	A19	**DIFF_n O**	U5-14
	A20	**DQ**	U5-13
	A22		D30
	B11	**DIFF_n O**	Open
	B12	**DQ**	U5-31
	B13	**DIFF_p O**	U5-29
	B15	**DQ**	U5-24
	B16		U5-21
	B17		U5-20
	B18	**DIFF_p O**	U5-19
	B19	VCCIO	3.3V
	B20	**DQ**	U5-12
	B21		D31
	B22		D29
	C11	**DQ**	Open
	C12	VCCIO	3.3V
	C13	**DQ**	Open
	C14	VREF	
	C15	**DQ**	U5-23
	C16		U5-22
	C18		U5-16
	C19		U5-15
	C20		U5-11
	C21		D28
	C22	VCCIO	3.3V
	D12	**DQ**	U5-37 (H16?)
	D13		Open
	D15	VCCIO	3.3V
	D17	**DQ**	Open
	D19		U5-10
	D21		D22
	D22		D26
	E12		U5-38
	E14		Open

FPGA			Board
IOBANK_7A	E15	**DQ**	U5-25
	E16		KEY2
	E18	VCCIO	3.3V
	E19	**DQ**	U5-9
	E20	**DIFF_p O**	D25
	E21	**DQ**	DQM3
	E22		D24
	F11	VCCIO	3.3V
	F12	**DQ**	Open
	F13		Open
	F14		U5-34
	F15		U5-26
	F17	GND for	GND
	F18	**DQSB**	U5-8
	F19	**DQS**	U5-7
	F20	**DQ**	Open
	F21	VCCIO	3.3V
	F22	**DIFF_n O**	D23
	G11	**DQ**	Open
	G12	**DQSB**	U5-40
	G13	**CLK_n**	U5-36
	G14	VCCIO	3.3V
	G15	**DQ**	U5-33
	G16		Open
	G17		SDCKE0
	G18	**DQS**	SDCLK0
	G20	**DIFF_p I**	Open
	G21	**DIFF_n I**	D27
	G22	**DQ**	D21
	H10	**DIFF_n O**	Open
	H11	**DQS**	U5-39
	H13	**CLK_p**	U5-35
	H14	**DQS**	Open
	H15	**CLK_n**	Open
	H16	**CLK_p**	(H16?)
	H17	VCCIO	3.3V
	H18	**DQSB**	A11
	H20	**DIFF_n I**	A12
	H21	**DIFF_p I**	D20
	J11	**DQ**	Open
	J13	**DQSB**	Open
	J17	**DQ**	KEY1

FPGA			Board
IOBANK_7A	J18	**DQ**	A8
	J19	**DIFF_p O**	A9
	J21	**DQS**	D19
	J22	**DQSB**	D18
	K9	**DQ**	Open
	K16		A6
	K19	**DIFF_n I**	Open
	K20	**DIFF_p I**	DQM2
	L8	**DIFF_p O**	Open
		80 I/Os	In I/O Out

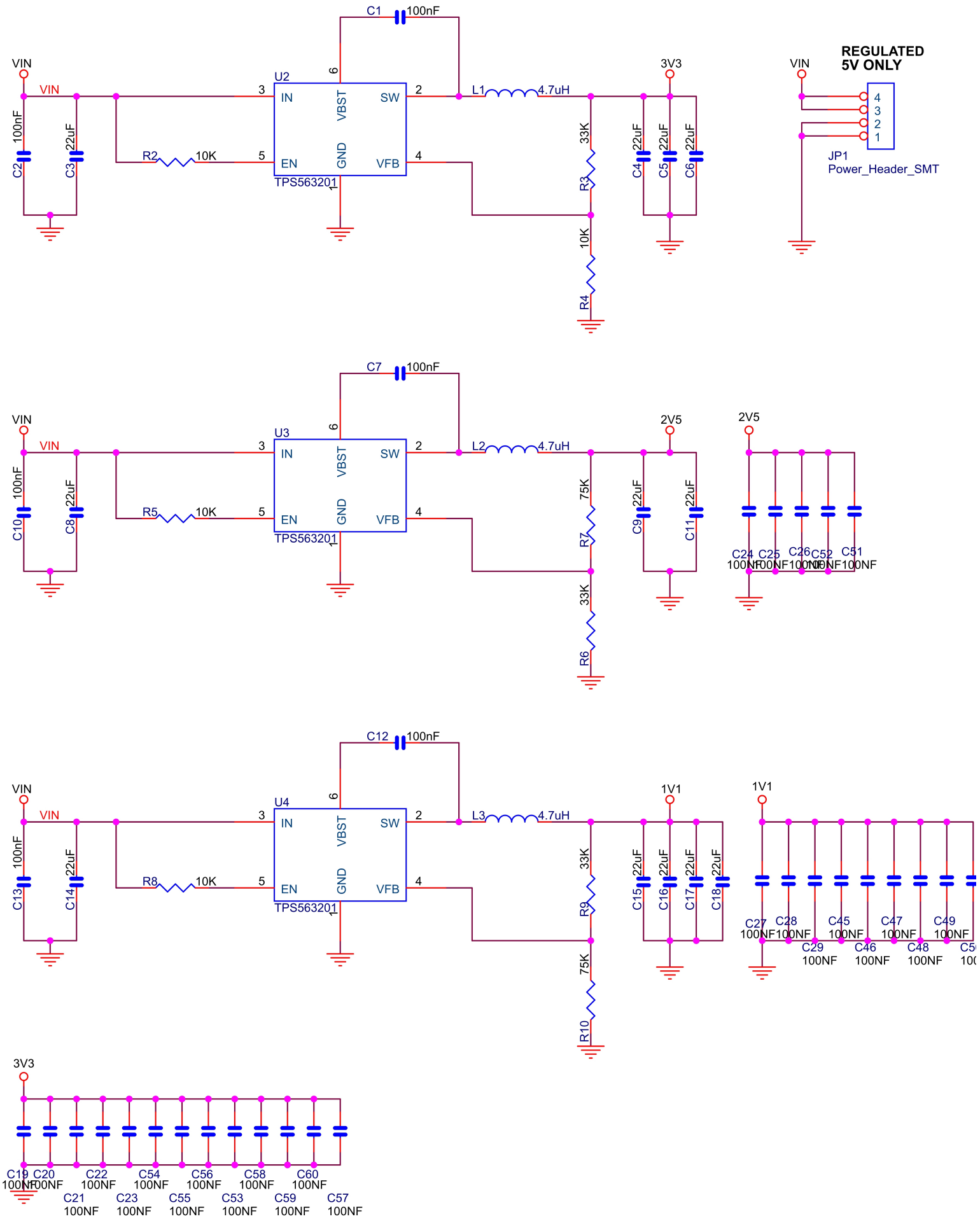
FPGA			Board
IOBANK_9A	A2	MSEL2	GND
	A4	nCONFIG	3.3V
	C5	GND for	GND
	E5	MSEL3	GND
	F3	MSEL4	3.3V
	G5	nCE	GND
	H5	nSTATUS	3.3V
	J6	MSEL1	3.3V
	K6	CONF_DONE	3.3V
	L6	MSEL0	3.3V
		0 I/Os	In I/O Out

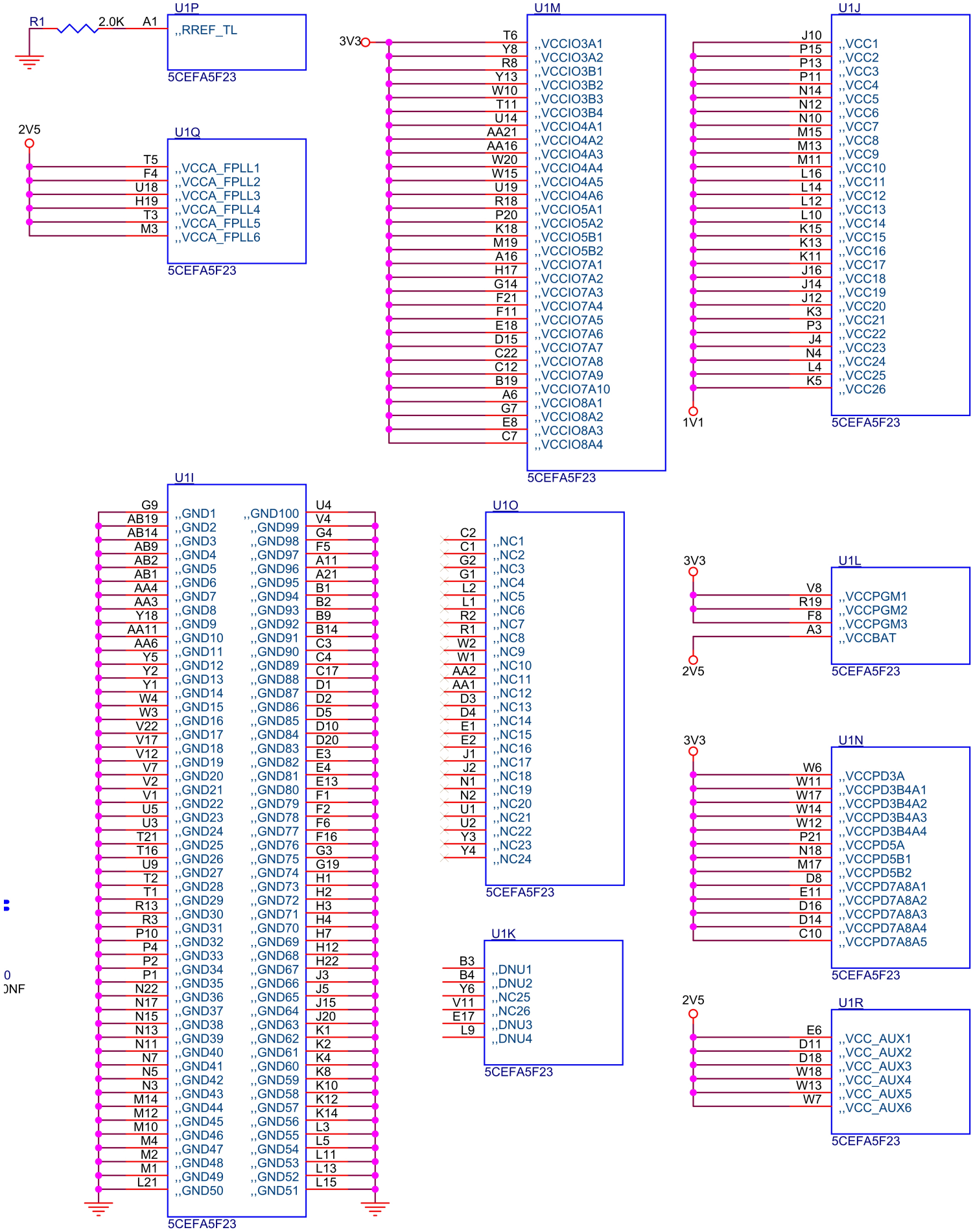
FPGA			Board
IOBANK_8A	A5	**DQ**	U5-59
	A6	VCCIO	3.3V
	A7	**DQ**	U5-54
	A8		U5-53
	A9		U5-42
	A10	**DIFF_p O**	U5-41
	B5	**DIFF_n O**	U5-60
	B6	**DQ**	U5-55
	B7		U5-56
	B8	VREF	GND
	B10	**DQ**	Open
	C6		U5-57
	C7	VCCIO	3.3V
	C8	**DQ**	Open
	C9		Open
	D6		U5-58
	D7	**DIFF_p O**	Open
	D9	**DQSB**	U5-46
	E7	**DIFF_n O**	Open
	E8	VCCIO	3.3V
	E9	**DQS**	U5-45
	E10	**CLK_p**	Open
	F7	**DQ**	Open
	F9	**CLK_n**	Open
	F10		Open
	G6	**DQ**	Open
	G7	VCCIO	3.3V
	G8	**PLL**	U5-48
	G10	**CLK_p**	Open
	H6	**DQ**	Open
	H8	**PLL**	U5-47
	H9	**DQSB**	U5-44
	J7	**DQ**	U5-51
	J8		U5-52
	J9	**DQS**	U5-43
	K7	**DQ**	U5-50
	L7		U5-49
		32 I/Os	In I/O Out

Each bank has independent power supplies (VCCIO; Vcc for I/Os and VCCPD; Vcc for I/O pads) to allow different I/O standards. All VCCIOs are connected to 3.3V.

IOBANK_	3A	3B	4A	5A	5B	7A	8A	**Total**
GPIO Pins	16	32	48	16	16	80	32	240

FPGA Board Schematics

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A1
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U1Q
2V5
T5
F4
U18
H19
T3
M3
,,VCCA_FPLL1
,,VCCA_FPLL2
,,VCCA_FPLL3
,,VCCA_FPLL4
,,VCCA_FPLL5
,,VCCA_FPLL6
5CEFA5F23
U1M
3V3
T6
Y8
R8
Y13
W10
T11
U14
AA21
AA16
W20
W15
U19
R18
P20
K18
M19
A16
H17
G14
F21
F11
E18
D15
C22
C12
B19
A6
G7
E8
C7
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AB9
AB2
AB1
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AA3
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AA11
AA6
Y5
Y2
Y1
W4
W3
V22
V17
V12
V7
V2
V1
U5
U3
T21
T16
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T2
T1
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R3
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P2
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V4
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F5
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B1
B2
B9
B14
C3
C4
C17
D1
D2
D5
D10
D20
E3
E4
E13
F1
F2
F6
F16
G3
G19
H1
H2
H3
H4
H7
H12
H22
J3
J5
J15
J20
K1
K2
K4
K8
K10
K12
K14
L3
L5
L11
L13
L15
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U1O
C2
C1
G2
G1
L2
L1
R2
R1
W2
W1
AA2
AA1
D3
D4
E1
E2
J1
J2
N1
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U1
U2
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Y4
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3V3
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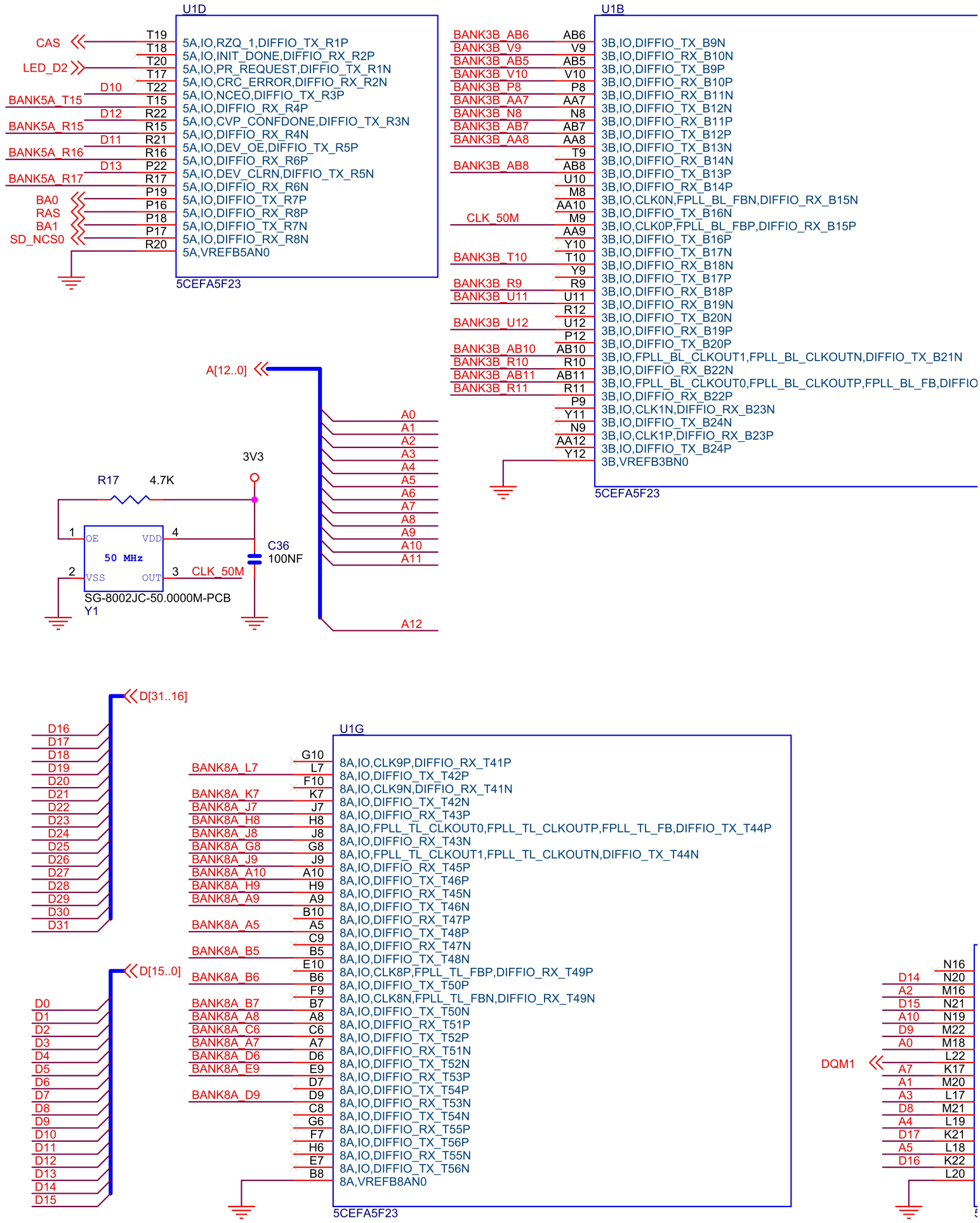
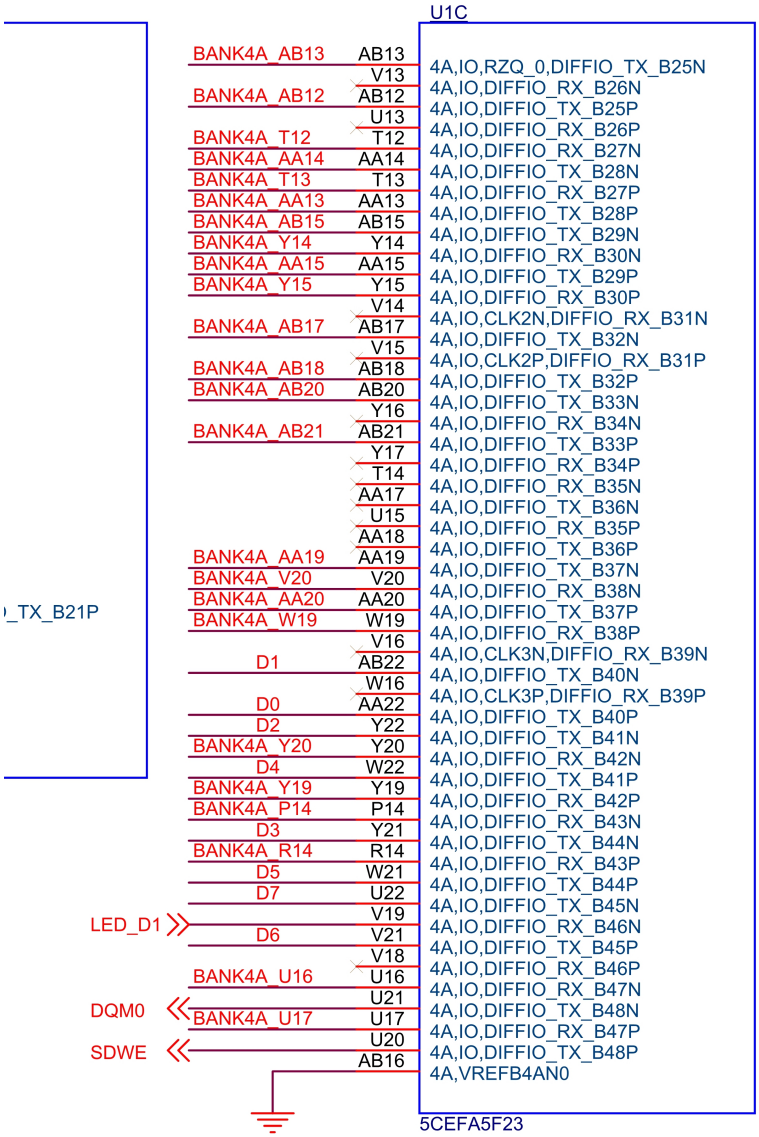
W12
P21
N18
M17
D8
E11
D16
D14
C10
,,VCCPD3A
,,VCCPD3B4A1
,,VCCPD3B4A2
,,VCCPD3B4A3
,,VCCPD3B4A4
,,VCCPD5A
,,VCCPD5B1
,,VCCPD5B2
,,VCCPD7A8A1
,,VCCPD7A8A2
,,VCCPD7A8A3
,,VCCPD7A8A4
,,VCCPD7A8A5
5CEFA5F23
2V5
U1R
E6
D11
D18
W18
W13
W7
,,VCC_AUX1
,,VCC_AUX2
,,VCC_AUX3
,,VCC_AUX4
,,VCC_AUX5
,,VCC_AUX6
5CEFA5F23


U1D
CAS
LED_D2
D10
BANK5A_T15
D12
BANK5A_R15
D11
BANK5A_R16
D13
BANK5A_R17
BA0
RAS
BA1
SD_NCS0
T19 5A,IO,RZQ_1,DIFFIO_TX_R1P
T18 5A,IO,INIT_DONE,DIFFIO_RX_R2P
T20 5A,IO,PR_REQUEST,DIFFIO_TX_R1N
T17 5A,IO,CRC_ERROR,DIFFIO_RX_R2N
T22 5A,IO,NCEO,DIFFIO_TX_R3P
T15 5A,IO,DIFFIO_RX_R4P
R22 5A,IO,CVP_CONFDONE,DIFFIO_TX_R3N
R15 5A,IO,DIFFIO_RX_R4N
R21 5A,IO,DEV_OE,DIFFIO_TX_R5P
R16 5A,IO,DIFFIO_RX_R6P
P22 5A,IO,DEV_CLRN,DIFFIO_TX_R5N
R17 5A,IO,DIFFIO_RX_R6N
P19 5A,IO,DIFFIO_TX_R7P
P16 5A,IO,DIFFIO_RX_R8P
P18 5A,IO,DIFFIO_TX_R7N
P17 5A,IO,DIFFIO_RX_R8N
R20 5A,VREFB5AN0
5CEFA5F23
U1B
BANK3B_AB6 AB6 3B,IO,DIFFIO_TX_B9N
BANK3B_V9 V9 3B,IO,DIFFIO_RX_B10N
BANK3B_AB5 AB5 3B,IO,DIFFIO_TX_B9P
BANK3B_V10 V10 3B,IO,DIFFIO_RX_B10P
BANK3B_P8 P8 3B,IO,DIFFIO_RX_B11N
BANK3B_AA7 AA7 3B,IO,DIFFIO_TX_B12N
BANK3B_N8 N8 3B,IO,DIFFIO_RX_B11P
BANK3B_AB7 AB7 3B,IO,DIFFIO_TX_B12P
BANK3B_AA8 AA8 3B,IO,DIFFIO_TX_B13N
T9 3B,IO,DIFFIO_RX_B14N
BANK3B_AB8 AB8 3B,IO,DIFFIO_TX_B13P
U10 3B,IO,DIFFIO_RX_B14P
M8 3B,IO,CLK0N,FPLL_BL_FBN,DIFFIO_RX_B15N
AA10 3B,IO,DIFFIO_TX_B16N
CLK_50M M9 3B,IO,CLK0P,FPLL_BL_FBP,DIFFIO_RX_B15P
AA9 3B,IO,DIFFIO_TX_B16P
Y10 3B,IO,DIFFIO_TX_B17N
BANK3B_T10 T10 3B,IO,DIFFIO_RX_B18N
Y9 3B,IO,DIFFIO_TX_B17P
BANK3B_R9 R9 3B,IO,DIFFIO_RX_B18P
BANK3B_U11 U11 3B,IO,DIFFIO_RX_B19N
R12 3B,IO,DIFFIO_TX_B20N
BANK3B_U12 U12 3B,IO,DIFFIO_RX_B19P
P12 3B,IO,DIFFIO_TX_B20P
BANK3B_AB10 AB10 3B,IO,FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTN,DIFFIO_TX_B21N
BANK3B_R10 R10 3B,IO,DIFFIO_RX_B22N
BANK3B_AB11 AB11 3B,IO,FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTP,FPLL_BL_FB,DIFFIO
BANK3B_R11 R11 3B,IO,DIFFIO_RX_B22P
P9 3B,IO,CLK1N,DIFFIO_RX_B23N
Y11 3B,IO,DIFFIO_TX_B24N
N9 3B,IO,CLK1P,DIFFIO_RX_B23P
AA12 3B,IO,DIFFIO_TX_B24P
Y12 3B,VREFB3BN0
5CEFA5F23
A[12..0]
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
3V3
R17 4.7K
1 OE
VDD 4
50 MHz
2 VSS
OUT 3 CLK_50M
SG-8002JC-50.0000M-PCB
Y1
C36
100NF
D[31..16]
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
D[15..0]
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
U1G
G10 8A,IO,CLK9P,DIFFIO_RX_T41P
BANK8A_L7 L7 8A,IO,DIFFIO_TX_T42P
F10 8A,IO,CLK9N,DIFFIO_RX_T41N
BANK8A_K7 K7 8A,IO,DIFFIO_TX_T42N
BANK8A_J7 J7 8A,IO,DIFFIO_RX_T43P
BANK8A_H8 H8 8A,IO,FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTP,FPLL_TL_FB,DIFFIO_TX_T44P
BANK8A_J8 J8 8A,IO,DIFFIO_RX_T43N
BANK8A_G8 G8 8A,IO,FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTN,DIFFIO_TX_T44N
BANK8A_J9 J9 8A,IO,DIFFIO_RX_T45P
BANK8A_A10 A10 8A,IO,DIFFIO_TX_T46P
BANK8A_H9 H9 8A,IO,DIFFIO_RX_T45N
BANK8A_A9 A9 8A,IO,DIFFIO_TX_T46N
B10 8A,IO,DIFFIO_RX_T47P
BANK8A_A5 A5 8A,IO,DIFFIO_TX_T48P
C9 8A,IO,DIFFIO_RX_T47N
BANK8A_B5 B5 8A,IO,DIFFIO_TX_T48N
E10 8A,IO,CLK8P,FPLL_TL_FBP,DIFFIO_RX_T49P
BANK8A_B6 B6 8A,IO,DIFFIO_TX_T50P
F9 8A,IO,CLK8N,FPLL_TL_FBN,DIFFIO_RX_T49N
BANK8A_B7 B7 8A,IO,DIFFIO_TX_T50N
BANK8A_A8 A8 8A,IO,DIFFIO_RX_T51P
BANK8A_C6 C6 8A,IO,DIFFIO_TX_T52P
BANK8A_A7 A7 8A,IO,DIFFIO_RX_T51N
BANK8A_D6 D6 8A,IO,DIFFIO_TX_T52N
BANK8A_E9 E9 8A,IO,DIFFIO_RX_T53P
D7 8A,IO,DIFFIO_TX_T54P
BANK8A_D9 D9 8A,IO,DIFFIO_RX_T53N
C8 8A,IO,DIFFIO_TX_T54N
G6 8A,IO,DIFFIO_RX_T55P
F7 8A,IO,DIFFIO_TX_T56P
H6 8A,IO,DIFFIO_RX_T55N
E7 8A,IO,DIFFIO_TX_T56N
B8 8A,VREFB8AN0
5CEFA5F23
N16
D14 N20
A2 M16
D15 N21
A10 N19
D9 M22
A0 M18
L22
DQM1
A7 K17
A1 M20
A3 L17
D8 M21
A4 L19
D17 K21
A5 L18
D16 K22
L20


U1C
BANK4A_AB13 AB13
V13
BANK4A_AB12 AB12
U13
BANK4A_T12 T12
BANK4A_AA14 AA14
BANK4A_T13 T13
BANK4A_AA13 AA13
BANK4A_AB15 AB15
BANK4A_Y14 Y14
BANK4A_AA15 AA15
BANK4A_Y15 Y15
V14
BANK4A_AB17 AB17
V15
BANK4A_AB18 AB18
BANK4A_AB20 AB20
Y16
BANK4A_AB21 AB21
Y17
T14
AA17
U15
AA18
BANK4A_AA19 AA19
BANK4A_V20 V20
BANK4A_AA20 AA20
BANK4A_W19 W19
V16
D1 AB22
W16
D0 AA22
D2 Y22
BANK4A_Y20 Y20
D4 W22
BANK4A_Y19 Y19
BANK4A_P14 P14
D3 Y21
BANK4A_R14 R14
D5 W21
D7 U22
V19
LED_D1
D6 V21
V18
BANK4A_U16 U16
U21
DQM0
BANK4A_U17 U17
U20
SDWE
AB16
4A,IO,RZQ_0,DIFFIO_TX_B25N
4A,IO,DIFFIO_RX_B26N
4A,IO,DIFFIO_TX_B25P
4A,IO,DIFFIO_RX_B26P
4A,IO,DIFFIO_RX_B27N
4A,IO,DIFFIO_TX_B28N
4A,IO,DIFFIO_RX_B27P
4A,IO,DIFFIO_TX_B28P
4A,IO,DIFFIO_TX_B29N
4A,IO,DIFFIO_RX_B30N
4A,IO,DIFFIO_TX_B29P
4A,IO,DIFFIO_RX_B30P
4A,IO,CLK2N,DIFFIO_RX_B31N
4A,IO,DIFFIO_TX_B32N
4A,IO,CLK2P,DIFFIO_RX_B31P
4A,IO,DIFFIO_TX_B32P
4A,IO,DIFFIO_TX_B33N
4A,IO,DIFFIO_RX_B34N
4A,IO,DIFFIO_TX_B33P
4A,IO,DIFFIO_RX_B34P
4A,IO,DIFFIO_RX_B35N
4A,IO,DIFFIO_TX_B36N
4A,IO,DIFFIO_RX_B35P
4A,IO,DIFFIO_TX_B36P
4A,IO,DIFFIO_TX_B37N
4A,IO,DIFFIO_RX_B38N
4A,IO,DIFFIO_TX_B37P
4A,IO,DIFFIO_RX_B38P
4A,IO,CLK3N,DIFFIO_RX_B39N
4A,IO,DIFFIO_TX_B40N
4A,IO,CLK3P,DIFFIO_RX_B39P
4A,IO,DIFFIO_TX_B40P
4A,IO,DIFFIO_TX_B41N
4A,IO,DIFFIO_RX_B42N
4A,IO,DIFFIO_TX_B41P
4A,IO,DIFFIO_RX_B42P
4A,IO,DIFFIO_RX_B43N
4A,IO,DIFFIO_TX_B44N
4A,IO,DIFFIO_RX_B43P
4A,IO,DIFFIO_TX_B44P
4A,IO,DIFFIO_TX_B45N
4A,IO,DIFFIO_RX_B46N
4A,IO,DIFFIO_TX_B45P
4A,IO,DIFFIO_RX_B46P
4A,IO,DIFFIO_RX_B47N
4A,IO,DIFFIO_TX_B48N
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4A,IO,DIFFIO_TX_B48P
4A,VREFB4AN0
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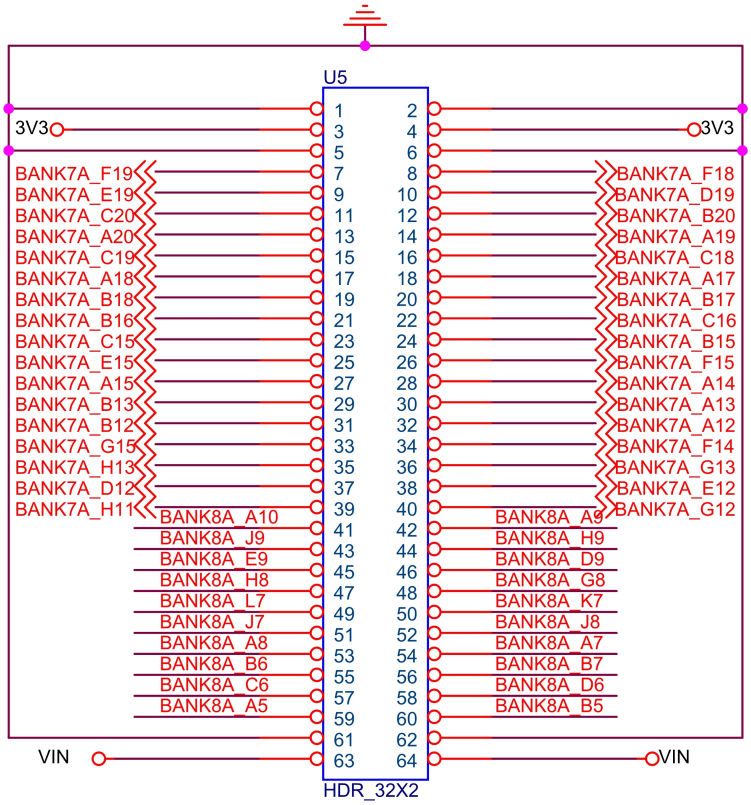
U5
3V3
BANK7A_F19
BANK7A_E19
BANK7A_C20
BANK7A_A20
BANK7A_C19
BANK7A_A18
BANK7A_B18
BANK7A_B16
BANK7A_C15
BANK7A_E15
BANK7A_A15
BANK7A_B13
BANK7A_B12
BANK7A_G15
BANK7A_H13
BANK7A_D12
BANK7A_H11
BANK8A_A10
BANK8A_J9
BANK8A_E9
BANK8A_H8
BANK8A_L7
BANK8A_J7
BANK8A_A8
BANK8A_B6
BANK8A_C6
BANK8A_A5
VIN
BANK7A_F18
BANK7A_D19
BANK7A_B20
BANK7A_A19
BANK7A_C18
BANK7A_A17
BANK7A_B17
BANK7A_C16
BANK7A_B15
BANK7A_F15
BANK7A_A14
BANK7A_A13
BANK7A_A12
BANK7A_F14
BANK7A_G13
BANK7A_E12
BANK7A_G12
BANK8A_A9
BANK8A_H9
BANK8A_D9
BANK8A_G8
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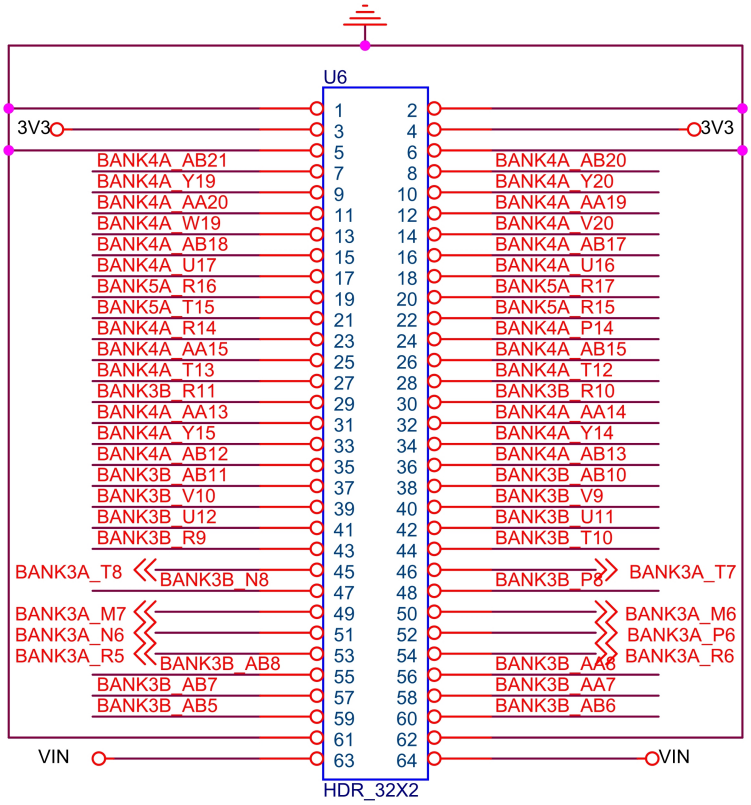
HDR_32X2


U6
3V3
BANK4A_AB21
BANK4A_Y19
BANK4A_AA20
BANK4A_W19
BANK4A_AB18
BANK4A_U17
BANK5A_R16
BANK5A_T15
BANK4A_R14
BANK4A_AA15
BANK4A_T13
BANK3B_R11
BANK4A_AA13
BANK4A_Y15
BANK4A_AB12
BANK3B_AB11
BANK3B_V10
BANK3B_U12
BANK3B_R9
BANK3A_T8
BANK3B_N8
BANK3A_M7
BANK3A_N6
BANK3A_R5
BANK3B_AB8
BANK3B_AB7
BANK3B_AB5
VIN
BANK4A_AB20
BANK4A_Y20
BANK4A_AA19
BANK4A_V20
BANK4A_AB17
BANK4A_U16
BANK5A_R17
BANK5A_R15
BANK4A_P14
BANK4A_AB15
BANK4A_T12
BANK3B_R10
BANK4A_AA14
BANK4A_Y14
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BANK3B_P8
BANK3A_T7
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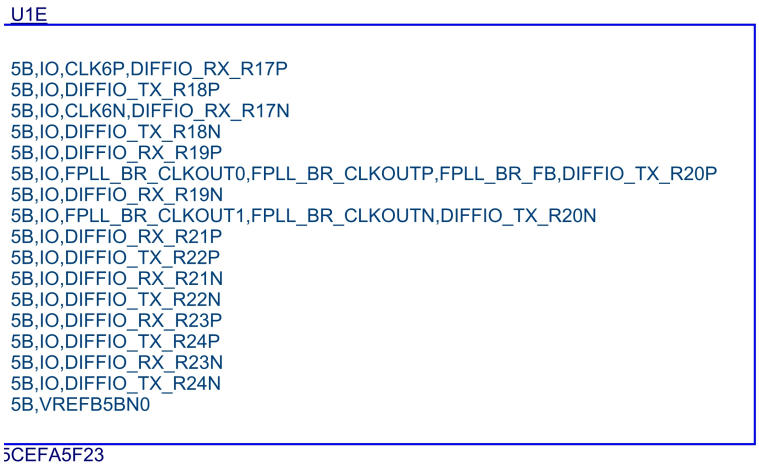
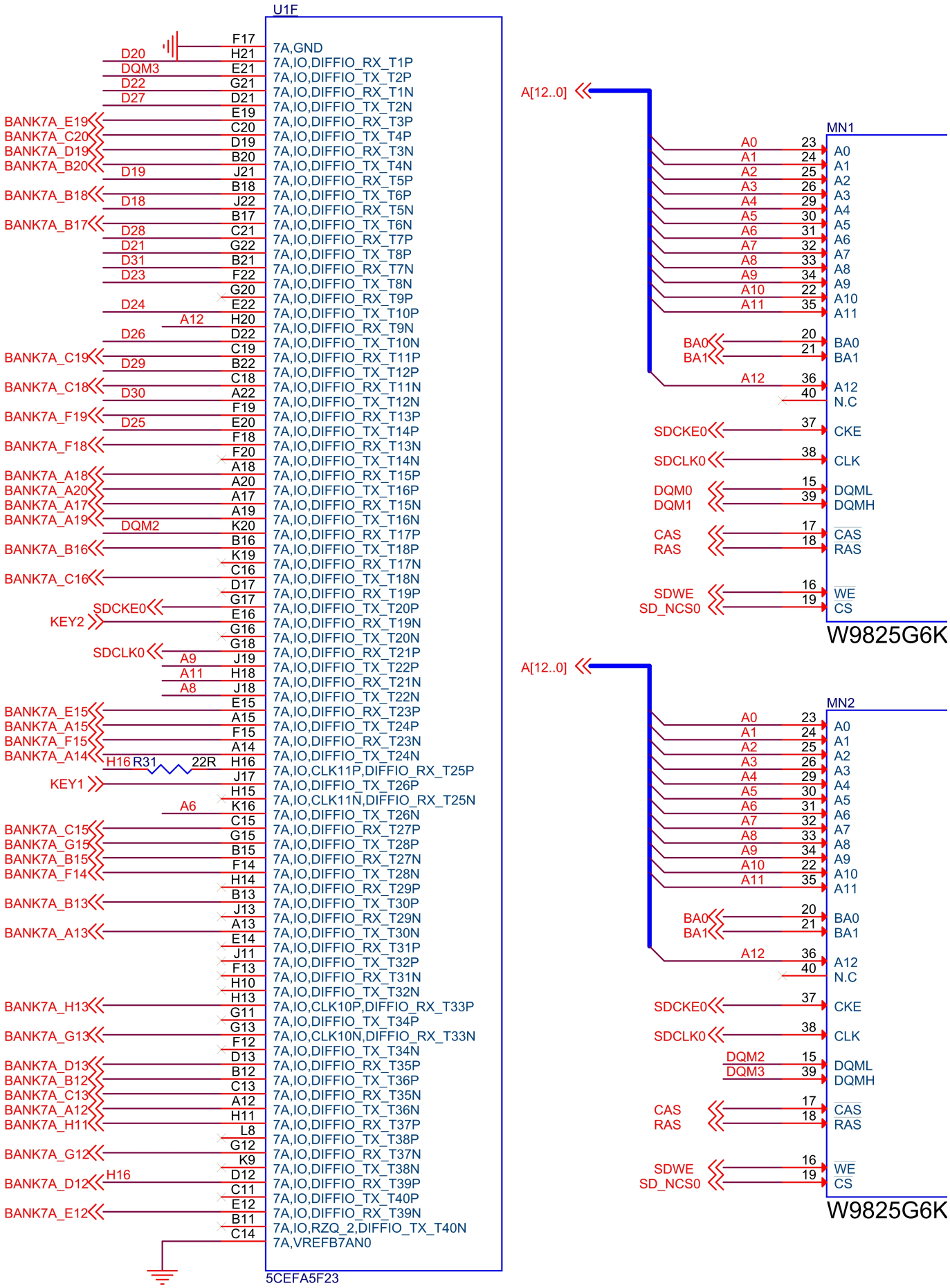
HDR_32X2


U1E
5B,IO,CLK6P,DIFFIO_RX_R17P
5B,IO,DIFFIO_TX_R18P
5B,IO,CLK6N,DIFFIO_RX_R17N
5B,IO,DIFFIO_TX_R18N
5B,IO,DIFFIO_RX_R19P
5B,IO,FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTP,FPLL_BR_FB,DIFFIO_TX_R20P
5B,IO,DIFFIO_RX_R19N
5B,IO,FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTN,DIFFIO_TX_R20N
5B,IO,DIFFIO_RX_R21P
5B,IO,DIFFIO_TX_R22P
5B,IO,DIFFIO_RX_R21N
5B,IO,DIFFIO_TX_R22N
5B,IO,DIFFIO_RX_R23P
5B,IO,DIFFIO_TX_R24P
5B,IO,DIFFIO_RX_R23N
5B,IO,DIFFIO_TX_R24N
5B,VREFB5BN0
5CEFA5F23


U1F
F17 7A,GND
D20 H21 7A,IO,DIFFIO_RX_T1P
DQM3 E21 7A,IO,DIFFIO_TX_T2P
D22 G21 7A,IO,DIFFIO_RX_T1N
D27 D21 7A,IO,DIFFIO_TX_T2N
BANK7A_E19 E19 7A,IO,DIFFIO_RX_T3P
BANK7A_C20 C20 7A,IO,DIFFIO_TX_T4P
BANK7A_D19 D19 7A,IO,DIFFIO_RX_T3N
BANK7A_B20 B20 7A,IO,DIFFIO_TX_T4N
D19 J21 7A,IO,DIFFIO_RX_T5P
BANK7A_B18 B18 7A,IO,DIFFIO_TX_T6P
D18 J22 7A,IO,DIFFIO_RX_T5N
BANK7A_B17 B17 7A,IO,DIFFIO_TX_T6N
D28 C21 7A,IO,DIFFIO_RX_T7P
D21 G22 7A,IO,DIFFIO_TX_T8P
D31 B21 7A,IO,DIFFIO_RX_T7N
D23 F22 7A,IO,DIFFIO_TX_T8N
G20 7A,IO,DIFFIO_RX_T9P
D24 E22 7A,IO,DIFFIO_TX_T10P
A12 H20 7A,IO,DIFFIO_RX_T9N
D26 D22 7A,IO,DIFFIO_TX_T10N
BANK7A_C19 C19 7A,IO,DIFFIO_RX_T11P
D29 B22 7A,IO,DIFFIO_TX_T12P
BANK7A_C18 C18 7A,IO,DIFFIO_RX_T11N
D30 A22 7A,IO,DIFFIO_TX_T12N
BANK7A_F19 F19 7A,IO,DIFFIO_RX_T13P
D25 E20 7A,IO,DIFFIO_TX_T14P
BANK7A_F18 F18 7A,IO,DIFFIO_RX_T13N
F20 7A,IO,DIFFIO_TX_T14N
BANK7A_A18 A18 7A,IO,DIFFIO_RX_T15P
BANK7A_A20 A20 7A,IO,DIFFIO_TX_T16P
BANK7A_A17 A17 7A,IO,DIFFIO_RX_T15N
BANK7A_A19 A19 7A,IO,DIFFIO_TX_T16N
DQM2 K20 7A,IO,DIFFIO_RX_T17P
BANK7A_B16 B16 7A,IO,DIFFIO_TX_T18P
K19 7A,IO,DIFFIO_RX_T17N
BANK7A_C16 C16 7A,IO,DIFFIO_TX_T18N
D17 7A,IO,DIFFIO_RX_T19P
SDCKE0 G17 7A,IO,DIFFIO_TX_T20P
KEY2 E16 7A,IO,DIFFIO_RX_T19N
G16 7A,IO,DIFFIO_TX_T20N
SDCLK0 G18 7A,IO,DIFFIO_RX_T21P
A9 J19 7A,IO,DIFFIO_TX_T22P
A11 H18 7A,IO,DIFFIO_RX_T21N
A8 J18 7A,IO,DIFFIO_TX_T22N
BANK7A_E15 E15 7A,IO,DIFFIO_RX_T23P
BANK7A_A15 A15 7A,IO,DIFFIO_TX_T24P
BANK7A_F15 F15 7A,IO,DIFFIO_RX_T23N
BANK7A_A14 A14 7A,IO,DIFFIO_TX_T24N
H16 R31 22R H16 7A,IO,CLK11P,DIFFIO_RX_T25P
KEY1 J17 7A,IO,DIFFIO_TX_T26P
H15 7A,IO,CLK11N,DIFFIO_RX_T25N
A6 K16 7A,IO,DIFFIO_TX_T26N
BANK7A_C15 C15 7A,IO,DIFFIO_RX_T27P
BANK7A_G15 G15 7A,IO,DIFFIO_TX_T28P
BANK7A_B15 B15 7A,IO,DIFFIO_RX_T27N
BANK7A_F14 F14 7A,IO,DIFFIO_TX_T28N
H14 7A,IO,DIFFIO_RX_T29P
BANK7A_B13 B13 7A,IO,DIFFIO_TX_T30P
J13 7A,IO,DIFFIO_RX_T29N
BANK7A_A13 A13 7A,IO,DIFFIO_TX_T30N
E14 7A,IO,DIFFIO_RX_T31P
J11 7A,IO,DIFFIO_TX_T32P
F13 7A,IO,DIFFIO_RX_T31N
H10 7A,IO,DIFFIO_TX_T32N
BANK7A_H13 H13 7A,IO,CLK10P,DIFFIO_RX_T33P
G11 7A,IO,DIFFIO_TX_T34P
BANK7A_G13 G13 7A,IO,CLK10N,DIFFIO_RX_T33N
F12 7A,IO,DIFFIO_TX_T34N
BANK7A_D13 D13 7A,IO,DIFFIO_RX_T35P
BANK7A_B12 B12 7A,IO,DIFFIO_TX_T36P
BANK7A_C13 C13 7A,IO,DIFFIO_RX_T35N
BANK7A_A12 A12 7A,IO,DIFFIO_TX_T36N
BANK7A_H11 H11 7A,IO,DIFFIO_RX_T37P
L8 7A,IO,DIFFIO_TX_T38P
BANK7A_G12 G12 7A,IO,DIFFIO_RX_T37N
K9 7A,IO,DIFFIO_TX_T38N
H16 BANK7A_D12 D12 7A,IO,DIFFIO_RX_T39P
C11 7A,IO,DIFFIO_TX_T40P
BANK7A_E12 E12 7A,IO,DIFFIO_RX_T39N
B11 7A,IO,RZQ_2,DIFFIO_TX_T40N
C14 7A,VREFB7AN0
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MN1
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A1 24 A1
A2 25 A2
A3 26 A3
A4 29 A4
A5 30 A5
A6 31 A6
A7 32 A7
A8 33 A8
A9 34 A9
A10 22 A10
A11 35 A11
BA0 20 BA0
BA1 21 BA1
A12 36 A12
40 N.C
SDCKE0 37 CKE
SDCLK0 38 CLK
DQM0 15 DQML
DQM1 39 DQMH
CAS 17 CAS
RAS 18 RAS
SDWE 16 WE
SD_NCS0 19 CS
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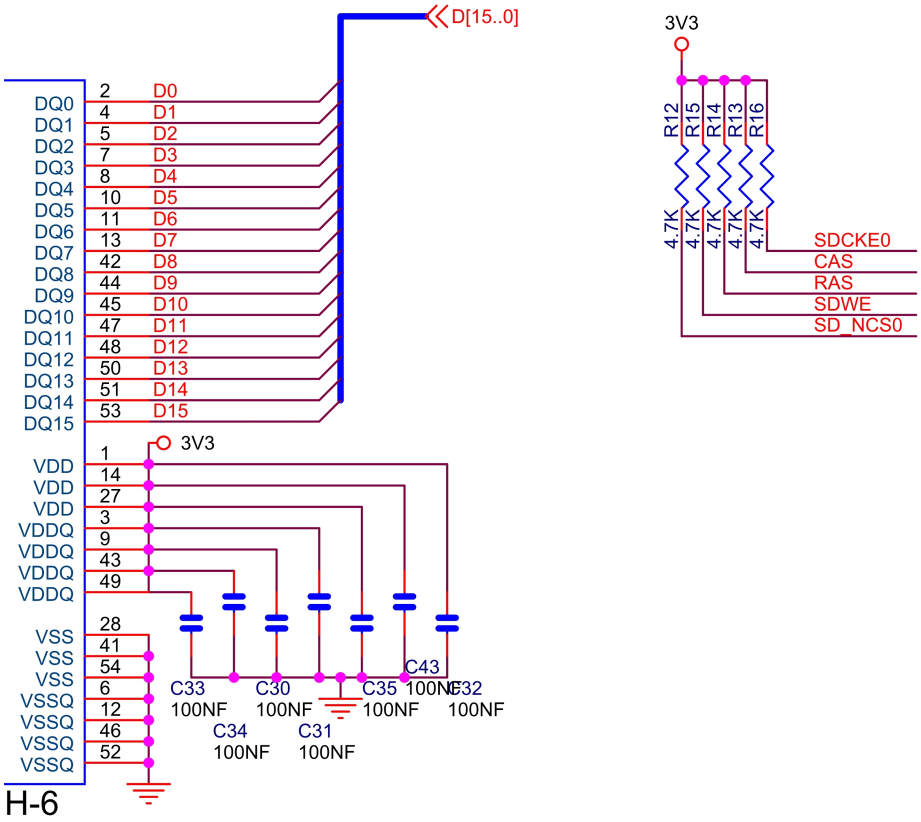
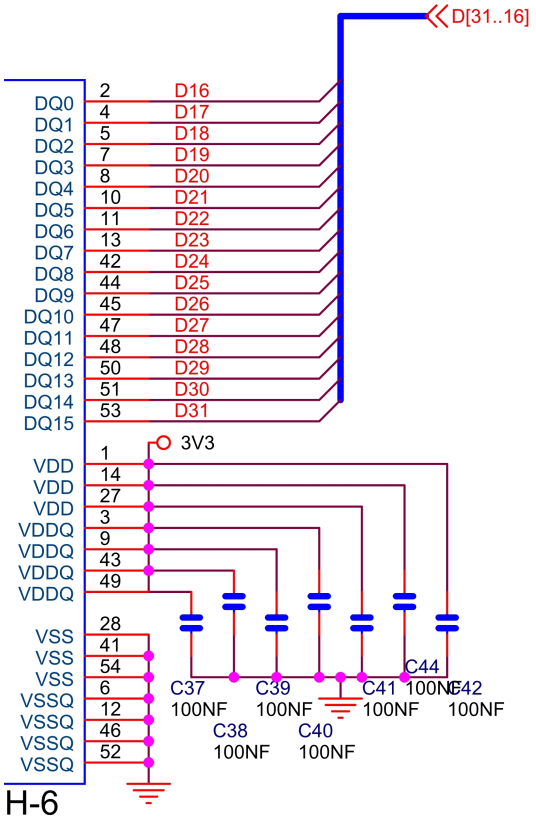
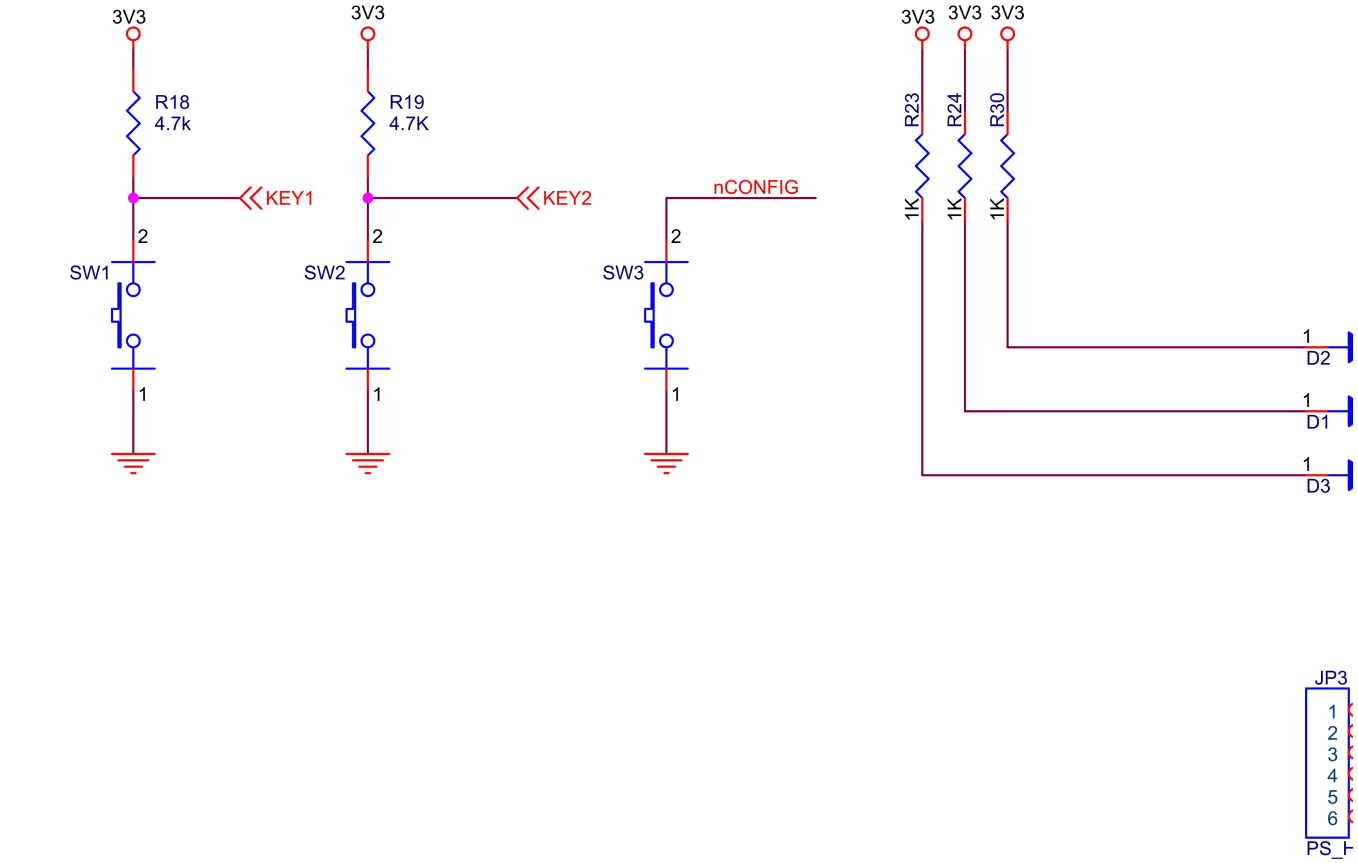
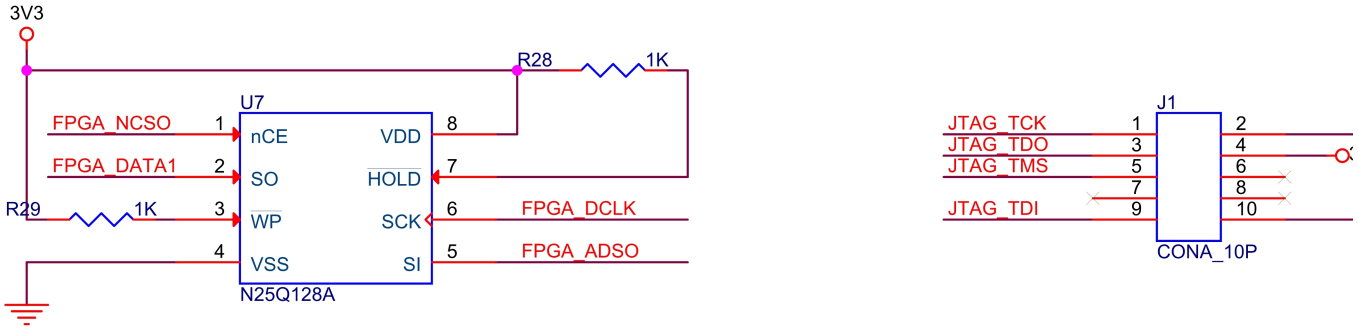
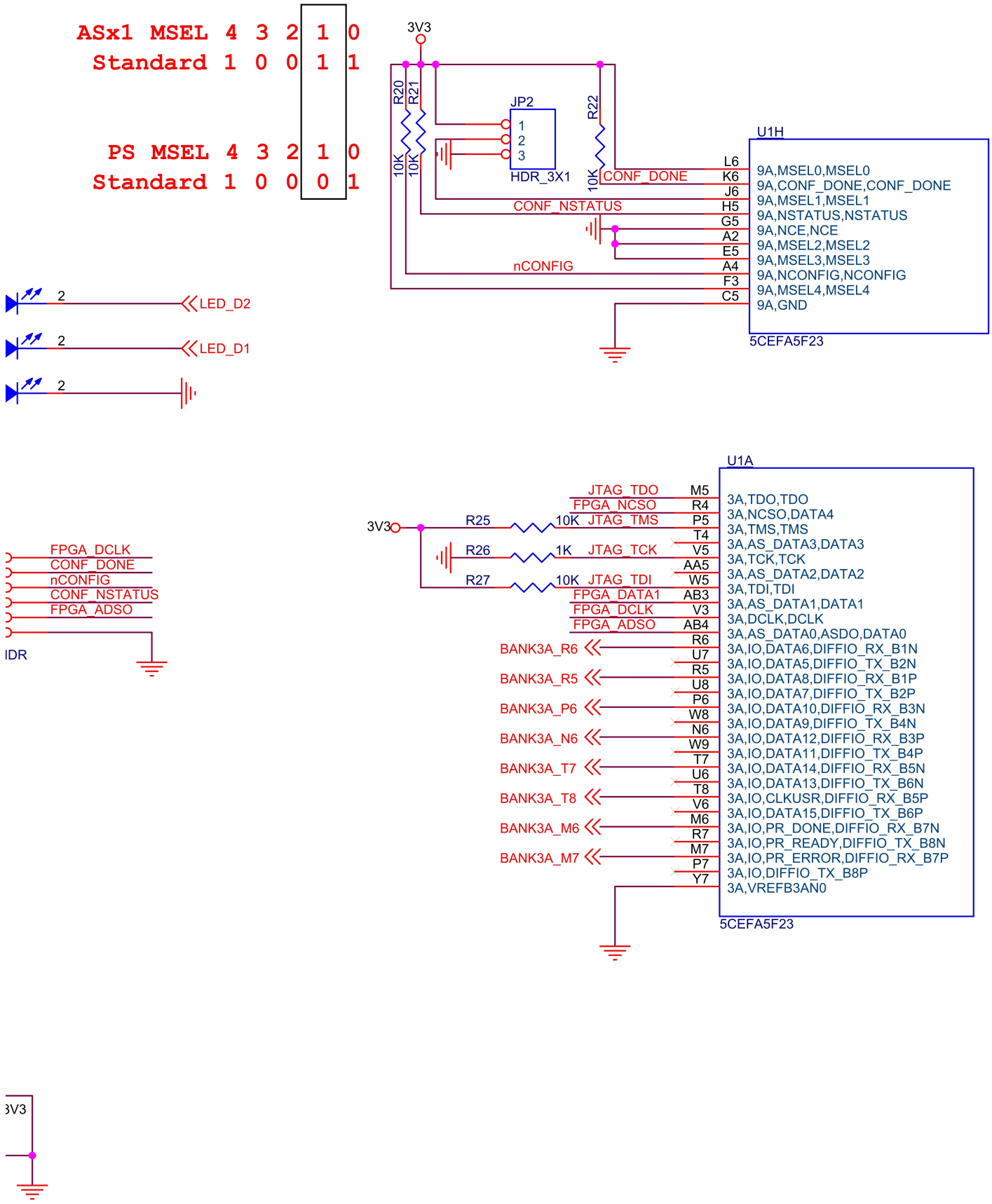
A1 24 A1
A2 25 A2
A3 26 A3
A4 29 A4
A5 30 A5
A6 31 A6
A7 32 A7
A8 33 A8
A9 34 A9
A10 22 A10
A11 35 A11
BA0 20 BA0
BA1 21 BA1
A12 36 A12
40 N.C
SDCKE0 37 CKE
SDCLK0 38 CLK
DQM2 15 DQML
DQM3 39 DQMH
CAS 17 CAS
RAS 18 RAS
SDWE 16 WE
SD_NCS0 19 CS
W9825G6K


D[15..0]
3V3
R12
R15
R14
R13
R16
4.7K
SDCKE0
CAS
RAS
SDWE
SD_NCS0
DQ0 2 D0
DQ1 4 D1
DQ2 5 D2
DQ3 7 D3
DQ4 8 D4
DQ5 10 D5
DQ6 11 D6
DQ7 13 D7
DQ8 42 D8
DQ9 44 D9
DQ10 45 D10
DQ11 47 D11
DQ12 48 D12
DQ13 50 D13
DQ14 51 D14
DQ15 53 D15
VDD 1
VDD 14
VDD 27
VDDQ 3
VDDQ 9
VDDQ 43
VDDQ 49
VSS 28
VSS 41
VSS 54
VSSQ 6
VSSQ 12
VSSQ 46
VSSQ 52
C33 100NF
C30 100NF
C35 100NF
C43 100NF
C32 100NF
C34 100NF
C31 100NF
H-6


D[31..16]
3V3
DQ0 2 D16
DQ1 4 D17
DQ2 5 D18
DQ3 7 D19
DQ4 8 D20
DQ5 10 D21
DQ6 11 D22
DQ7 13 D23
DQ8 42 D24
DQ9 44 D25
DQ10 45 D26
DQ11 47 D27
DQ12 48 D28
DQ13 50 D29
DQ14 51 D30
DQ15 53 D31
VDD 1
VDD 14
VDD 27
VDDQ 3
VDDQ 9
VDDQ 43
VDDQ 49
VSS 28
VSS 41
VSS 54
VSSQ 6
VSSQ 12
VSSQ 46
VSSQ 52
C37 100NF
C39 100NF
C41 100NF
C44 100NF
C42 100NF
C38 100NF
C40 100NF
H-6


3V3
R18
4.7k
KEY1
SW1
3V3
R19
4.7K
KEY2
SW2
nCONFIG
SW3
3V3 3V3 3V3
R23
R24
R30
1K
1K
1K
D2
D1
D3
JP3
PS_H


3V3
R28
1K
U7
FPGA_NCSO
FPGA_DATA1
R29
1K
nCE
SO
WP
VSS
VDD
HOLD
SCK
SI
FPGA_DCLK
FPGA_ADSO
N25Q128A
J1
JTAG_TCK
JTAG_TDO
JTAG_TMS
JTAG_TDI
CONA_10P


ASx1 MSEL 4 3 2 1 0
Standard 1 0 0 1 1
PS MSEL 4 3 2 1 0
Standard 1 0 0 0 1
3V3
R20
R21
10K
10K
JP2
1
2
3
HDR_3X1
R22
10K
CONF_DONE
CONF_NSTATUS
nCONFIG
U1H
L6
K6
J6
H5
G5
A2
E5
A4
F3
C5
9A,MSEL0,MSEL0
9A,CONF_DONE,CONF_DONE
9A,MSEL1,MSEL1
9A,NSTATUS,NSTATUS
9A,NCE,NCE
9A,MSEL2,MSEL2
9A,MSEL3,MSEL3
9A,NCONFIG,NCONFIG
9A,MSEL4,MSEL4
9A,GND
5CEFA5F23
2
LED_D2
2
LED_D1
2
FPGA_DCLK
CONF_DONE
nCONFIG
CONF_NSTATUS
FPGA_ADSO
IDR
3V3
R25
10K
JTAG_TMS
R26
1K
JTAG_TCK
R27
10K
JTAG_TDI
U1A
JTAG_TDO
FPGA_NCSO
FPGA_DATA1
FPGA_DCLK
FPGA_ADSO
BANK3A_R6
BANK3A_R5
BANK3A_P6
BANK3A_N6
BANK3A_T7
BANK3A_T8
BANK3A_M6
BANK3A_M7
M5
R4
P5
T4
V5
AA5
W5
AB3
V3
AB4
R6
U7
R5
U8
P6
W8
N6
W9
T7
U6
T8
V6
M6
R7
M7
P7
Y7
3A,TDO,TDO
3A,NCSO,DATA4
3A,TMS,TMS
3A,AS_DATA3,DATA3
3A,TCK,TCK
3A,AS_DATA2,DATA2
3A,TDI,TDI
3A,AS_DATA1,DATA1
3A,DCLK,DCLK
3A,AS_DATA0,ASDO,DATA0
3A,IO,DATA6,DIFFIO_RX_B1N
3A,IO,DATA5,DIFFIO_TX_B2N
3A,IO,DATA8,DIFFIO_RX_B1P
3A,IO,DATA7,DIFFIO_TX_B2P
3A,IO,DATA10,DIFFIO_RX_B3N
3A,IO,DATA9,DIFFIO_TX_B4N
3A,IO,DATA12,DIFFIO_RX_B3P
3A,IO,DATA11,DIFFIO_TX_B4P
3A,IO,DATA14,DIFFIO_RX_B5N
3A,IO,DATA13,DIFFIO_TX_B6N
3A,IO,CLKUSR,DIFFIO_RX_B5P
3A,IO,DATA15,DIFFIO_TX_B6P
3A,IO,PR_DONE,DIFFIO_RX_B7N
3A,IO,PR_READY,DIFFIO_TX_B8N
3A,IO,PR_ERROR,DIFFIO_RX_B7P
3A,IO,DIFFIO_TX_B8P
3A,VREFB3AN0
5CEFA5F23
3V3