NEC

NEC Electronics Inc.

μPD72120
Advanced Graphics Display Controller

Description

The μPD72120 Advanced Graphics Display Controller (AGDC) displays characters and graphics on a raster scan device from commands and parameters received from a host processor or CPU. Features of the AGDC include high-speed graphics drawing capabilities, video timing signal generation, large capacity display memory control (including video RAMs), and a versatile CPU interface. These features allow the AGDC to control graphics drawing and display of bit-mapped systems.

Features

- High-speed graphics drawing functions
  - Graphics drawing: dot, straight line, rectangle, circle, arc, sector, segment, ellipse, ellipse arc, ellipse sector, and ellipse segment
  - Maximum drawing speed
    500 ns/pixel (8 MHz, pixel mode)
    500 ns/dot (8 MHz, plane mode)
  - Area filling (high-speed processing in word units): triangle, trapezoid, circle, ellipse, and rectangle
  - Painting: filling of any arbitrary enclosed area (bit boundary retrieval)
  - Data transfers in display memory: multiplane transfers; data transformation (90°/180°/270° rotation and reversal); multiwindow transfers; maximum transfer speed of 500 ns/word
  - Image processing: slant, arbitrary angle rotation, 16/N enlargement, and N/16 shrinkage (N any integer from 1 to16)
  - Position specification by X-Y coordinates
  - Logical operations between planes
- Video timing signal generation
  - High-speed processing by two system clocks: display (for video sync signal generation) and graphics drawing clocks
  - External synchronization capability
- Large-capacity display memory
  - Display memory bus interface: 24-bit address and 16-bit data bus for addressing up to 16M words, 16 bits/word
  - Video RAM (VRAM) control
  - Display memory bus arbitration
- Host processor (CPU) interface
  - System bus interface: 20-bit address bus, 8- or 16-bit data bus
  - Data transfer with external DMA controller: from system memory to display memory (PUT); from display memory to system memory (GET)
  - High-speed pipeline processing with preprocessor before drawing processor
  - CPU memory or I/O mapping of internal registers and display memory for efficient system interface
- 8-MHz system clock
- CMOS technology
- Single +5-volt power supply
- Packages: 84-pin PLCC, 94-pin plastic miniflat

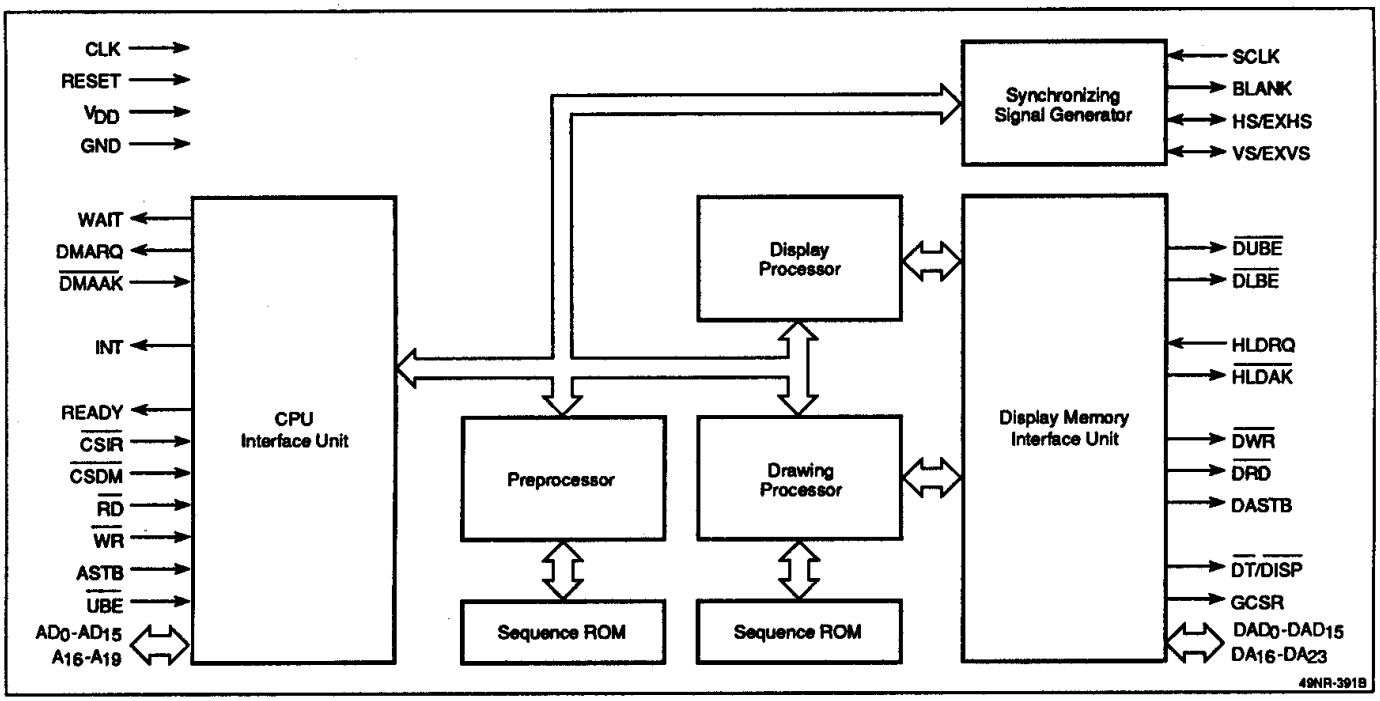
Ordering Information

Part No	Package
μPD72120L	84-pin PLCC
μPD72120GJ-5BG	94-pin plastic miniflat

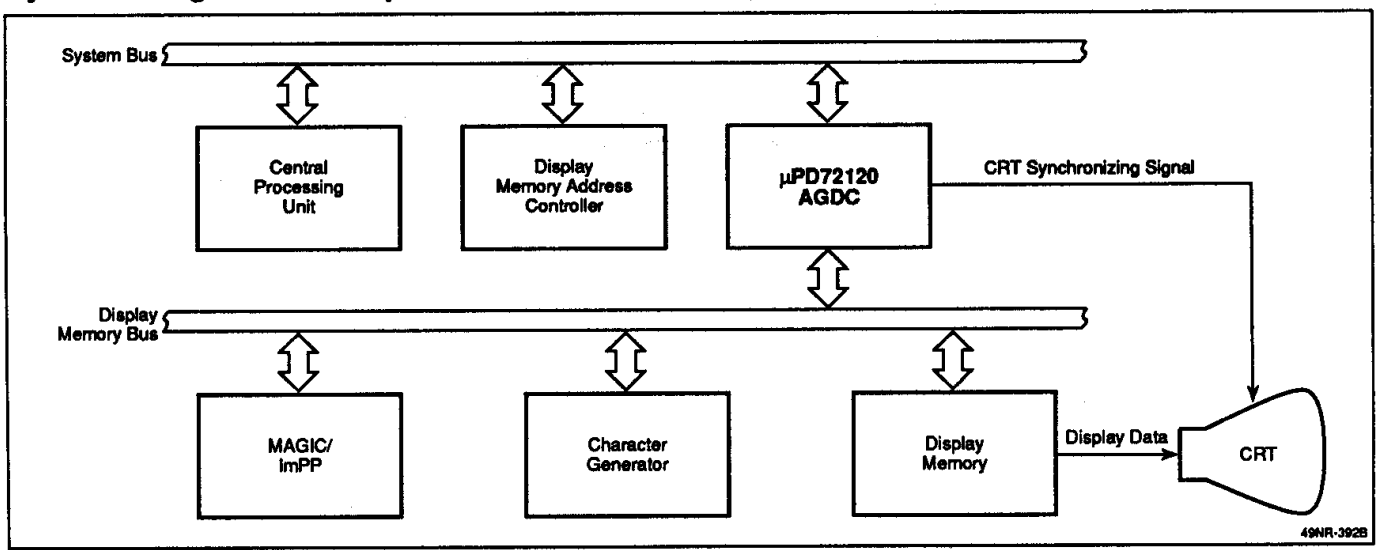
Pin Identification

Symbol	I/O	Signal Function
Clock Pins		
CLK	In	Clock supplied to circuits other than the sync signal generator and display processor. The drawing processor and preprocessor speed depend on this clock frequency.
SCLK	In	Clock supplied to the sync signal generator and the display processor. This clock frequency is determined by the CRT timing requirements: horizontal sync frequency, number of dots per line, etc.
System Bus Control Pins		
AD_0-AD_{15}	I/O	I/O bus to the CPU consisting of multiplexed 16-bit address and a bidirectional data bus.
A_{16}-A_{19}	In	Upper four address bits of the 20-bit address.
ASTB	In	Latches the address on A_{16}-A_{19} and AD_0-AD_{15} on the falling edge.
$\overline{UBE}$	In	Together with AD_0, defines the data access format as shown below. $\overline{UBE}$ should be tied high when connected to an 8-bit CPU. AD_0 $\overline{UBE}$ Data Access Format 0 0 Even-address word 0 1 Even-address byte 1 0 Odd-address byte 1 1 Odd-address byte
$\overline{RD}$	In	Performs a read of data from the AGDC by the host CPU.
$\overline{WR}$	In	Performs a write of data to the AGDC from the host CPU.
$\overline{CSIR}$	In	Enables reading/writing of the AGDC internal registers by the host CPU. The register is selected by the address input on AD_0-AD_7.
$\overline{CSDM}$	In	Enables reading/writing of display memory through the AGDC by the host CPU. The display memory address is generated by the address input on A_{16}-A_{19} and AD_0-AD_{15} and by the bank register.
READY	Out	Activated by the data access request ($\overline{RD}$/$\overline{WR}$) for the AGDC. During the access, the signal may be low. RESET will set the READY line high.
INT	Out	Signals an interrupt from the AGDC.
DMARQ	Out	Indicates a request for data transfer (PUT/GET) to an external DMA controller. DMARQ will be low after RESET.
$\overline{DMAAK}$	In	Acknowledgment of DMA request to the AGDC by the DMA controller.
RESET	In	Initializes operation of the AGDC. The internal parameter register is not cleared by RESET (it is initialized by setting data).
Display Memory Control Pins		
DAD_0-DAD_{15}	I/O	I/O pins for display memory; 16-bit address multiplexed with data.
DA_{16}-DA_{23}	Out	Upper 8 bits of display memory address (the lower 16 bits of the 24-bit address are output on DAD_0-DAD_{15}).
DASTB	Out	Indicates that a display memory address is present on the falling edge.
$\overline{DUBE}$, $\overline{DLBE}$	Out	Defines the data format for accessing the display. RESET sets both pins low. $\overline{DUBE}$ $\overline{DLBE}$ Data Access Format AGDC 0 0 Word 16-bit CPU 0 0 Word 8/16-bit CPU 0 1 High (odd) byte 8/16-bit CPU 1 0 Low (even) byte 8-bit CPU 1 1 High (odd) byte
$\overline{DRD}$	Out	Controls reading of the display memory by the AGDC. Set high by RESET.
$\overline{DWR}$	Out	Controls writing to the display memory by the AGDC. Set high by RESET.
HLDRQ	In	Requests control of the display memory bus by an external device to transfer display data.
$\overline{HLDAK}$	Out	Indicates that the AGDC memory bus (DAD_0-DAD_{15} and DA_{16}-DA_{23} is in high-impedance state so that an external device can have access to the display memory bus. Set high by RESET.
Video Timing Signal Related Pins		
VS/EXVS	I/O	When the AGDC operates as the master, VS is the vertical sync signal output. When the AGDC operates as a slave, the EXVS input initializes the internal vertical sync signal on the rising edge.
HS/EXHS	I/O	When the AGDC operates as the master, HS is the horizontal sync signal output. When the AGDC operates as a slave, EXHS initializes the internal horizontal sync signal on the rising edge.
Display Signal Related Pins		
BLANK	Out	Used to blank the display.
$\overline{DT/DISP}$	Out	Set to DT in the DT mode (when using VRAMs) and specifies the data transfer. In the cycle steal mode (VRAMs not used), indicates the display cycle.
GCSR	Out	Specifies the display of the graphics cursor
GWAIT	Out	Graphics wait signal
Other Pins		
V_{DD}		+5-volt power supply
GND		Ground
IC		Internally connected; leave unconnected

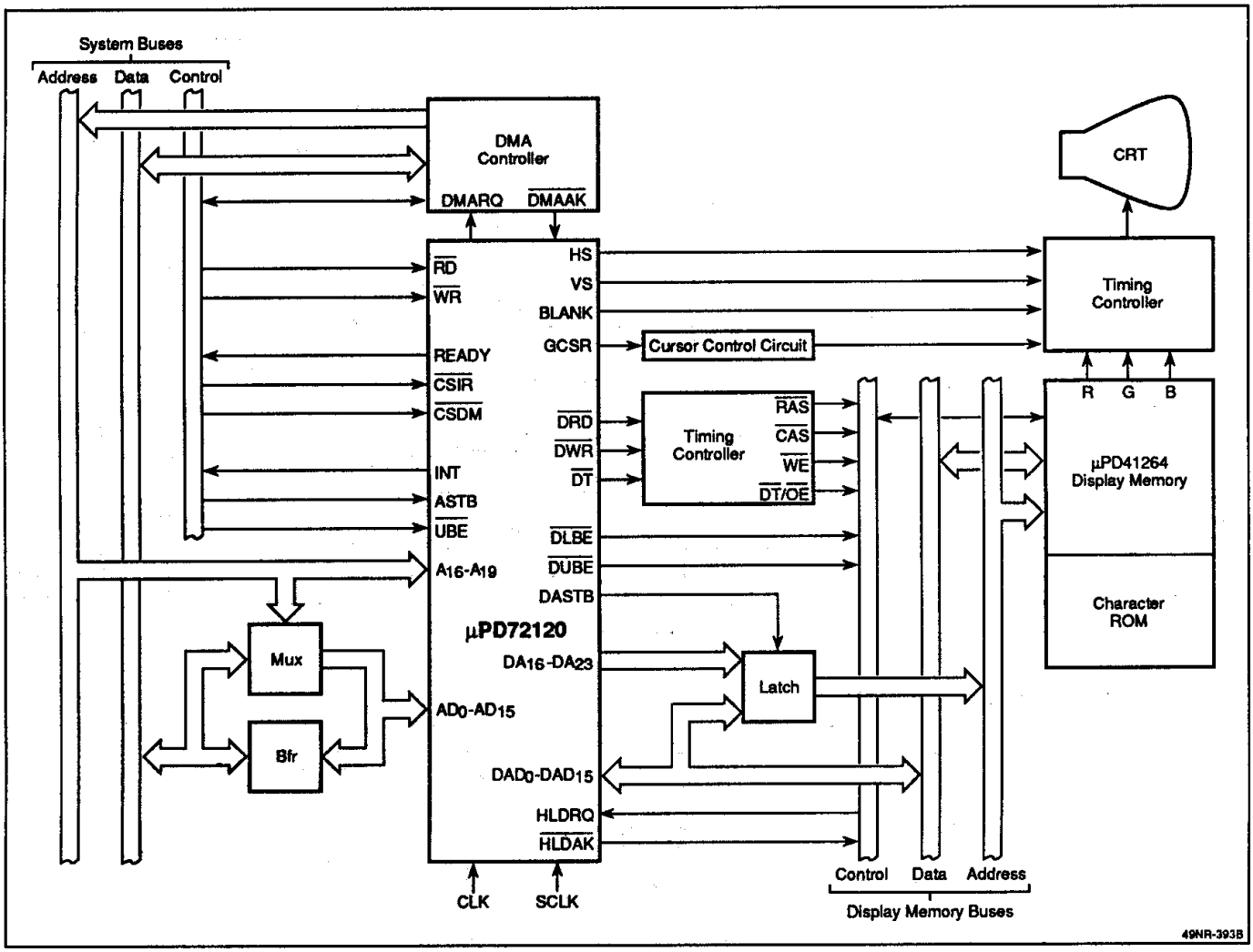
μPD72120 Block Diagram



System Configuration Example



General Application Diagram



Pin Configurations

84-Pin PLCC