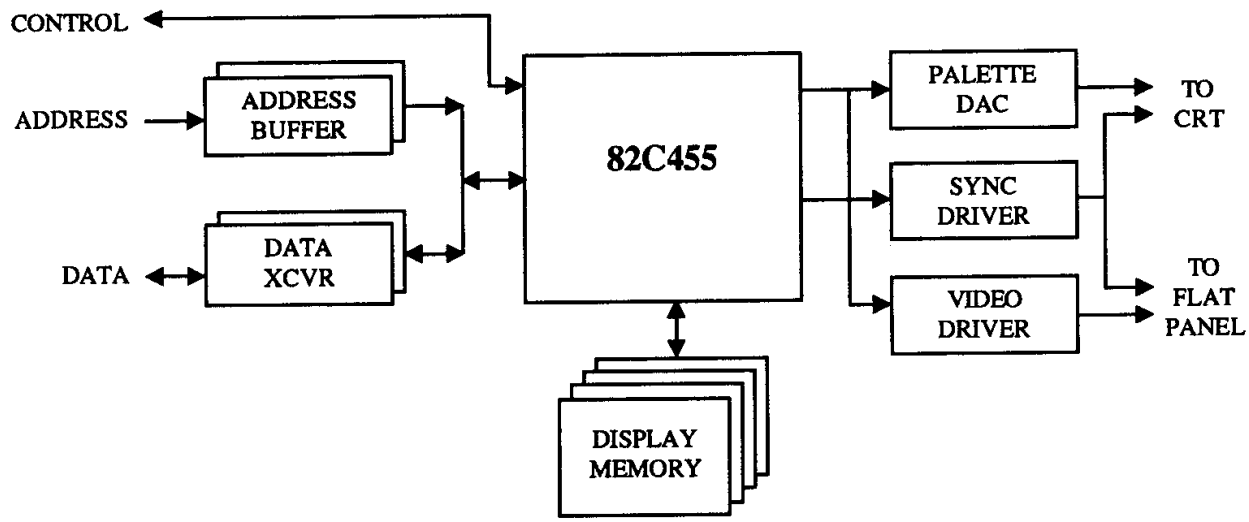
82C455
Flat Panel/CRT
VGA Controller

- 100% IBM VGA-compatible
- Supports analog/digital CRT monitors and LCD, Plasma, and Electro Luminescent panels of varying resolutions
- Up to 16 gray levels on monochrome panels
- Integrates full support of color panels
- Programmable vertical compensation techniques increase usable display area
- SMARTMAP™ intelligent color to gray level conversion
- Advanced SLEEP modes minimize power consumption
- Single chip implementation tightly couples to the CHIPS/280 and interfaces with 8- and 16-bit PC bus and MCA (an interface compatible with MicroChannel™)
- Can utilize an external palette DAC with up to 16 million colors
- Full backwards compatibility with IBM EGA, CGA, MDA and Hercules graphics standards



82C455 System Implementation

Introduction

The 82C455 VGA Flat Panel/CRT controller provides a single-chip solution for a VGA, EGA, CGA, MDA, or Hercules compatible display system. The 82C455 supports a wide variety of flat panel displays and CRT monitors.

By providing a high level of integration, the 82C455 minimizes the total chip count for VGA display subsystems. The 82C455's power-down features reduce power consumption of the display subsystem and extend battery life in portable applications. The 82C455 provides a variety of programmable features, such as Vertical Compensation, SMARTMAP™ and Alternate Registers to enhance the flat panel display.

FLAT PANEL DISPLAYS

There is currently no standard interface for flat panel displays. Interface signals and timing requirements vary between panel technologies and manufacturers. The 82C455 provides register programmable features to allow interfacing to the widest possible range of flat panel display units.

The 82C455 interfaces directly to monochrome, grayscale or color panels. A proprietary Frame Rate Control algorithm generates 16 gray levels on monochrome panels. (Frame Rate Control generates gray levels on monochrome panels by turning the pixels on and off over several frames.) The 82C455 outputs 16 level grayscale for panels which internally generate gray levels and drives color panels with up to 64 colors.

The 82C455 supports all flat panel display technologies including plasma, electroluminescent (EL) and liquid crystal displays (LCD). LCD panel interfaces are provided for single panel-single drive (SS), dual panel-single drive (DS), and dual panel dual drive (DD) configurations. A single panel sequences data similar to a CRT. In contrast, a dual panel requires video data sequence from separate locations in memory. In addition, a dual drive panel requires the sequence to occur simultaneously. The 82C455 handles the display data sequencing transparent to the application software providing full compatibility on both CRT and flat panel displays.

The 82C455 can support the popular panel resolutions of 640x200, 640x350, 640x400 and 640x480. For non-standard applications additional resolutions are supported. The 82C455 provides a direct interface to panels from vendors such as Sharp, Sanyo, Epson, Oki, Toshiba, Hitachi, Fujitsu, NEC, Matsushita and Finlux.

CRT MONITOR

The 82C455 supports both fixed and variable frequency analog monitors, including IBM PS/2™ and Multisync™ or Multi-Scan monitors. With the addition of a single CMOS PAL and required oscillators, the 82C455 supports digital TTL monitors for CGA, MDA and EGA standards. High resolution support is provided on both fixed and variable frequency monitors. When booting a system, the BIOS determines the monitor type and whether to boot on the CRT or flat panel. Programming a single register switches the display between the CRT and flat panel.

COMPATIBILITY

The 82C455 is fully compatible with the IBM VGA standard. The 82C455 also provides compatibility with IBM's EGA, CGA and MDA standard and the Hercules graphics adapter. The 82C455 includes a variety of features to provide compatibility on flat panel displays. Internal compensation techniques ensure that industry-standard software designed for different displays can be executed on the single flat panel used in an implementation. Mode initialization is supported at the BIOS and register levels, ensuring compatibility with all application software.

EXTENSION REGISTERS

The 82C455 employs an "Extension" Register set to control its enhanced features. These Extension Registers provide control of the flat panel interface, flat panel timing, vertical compensation, SMARTMAP™ and Backwards Compatibility.

Flat Panel Interface Registers

The Flat Panel Interface characteristics are controlled by a subset of the Extension Registers. These Registers select the panel type, data formatting, panel configuration, panel size, clock selection and video polarity. Since the 82C455 is designed to support a wide range of panel types and sizes, the control of these features is fully programmable. The video polarity of text and graphics modes is independently settable to allow black text on a white background and still provide normal graphics images.

Flat Panel Timing Registers

Flat panel displays usually require sync signal timing that is different from a CRT. To provide full compatibility with IBM VGA standard, alternate timing registers are used to allow independent timing of the sync signals for flat panel displays. Unlike the values programmed into the standard CRT timing registers, the value programmed into the alternate timing registers is dependent on the panel type used and is independent of the display mode.

VERTICAL COMPENSATION

Vertical Compensation is a programmable feature that increases the usable display area when running lower resolution software on a higher resolution panel. Unlike CRT monitors, flat panels have a fixed number of scan lines (e.g., 200, 350, 400 or 480 lines). Lower resolution software run on a higher resolution panel only partially fills the usable display area. For instance, 350-line EGA software displayed on a 480-line panel would leave 130 blank lines at the bottom of the display. The 82C455 offers the following three Vertical Compensation techniques to increase the useable screen area:

First, border insertion (referred to as "centering") adjusts the Display Start and Display End addresses to center the display, leaving a border of unused area at the top and bottom of the panel. Border insertion can be used in text and graphics modes.

Second, line replication (referred to as "stretching") duplicates every Nth display line (where N is programmable), thus stretching text characters and graphic images an adjustable amount. The display can be stretched to completely fill the flat panel area. Double scanning, a form of line replication where every line is replicated, is useful for running 200 line software on a 400 line panel. Line replication can be used in text and graphics modes.

Third, blank line insertion, inserts N blank lines (where N is programmable) between each line of text characters. Thus text can be evenly spaced to fill the entire panel display area without altering the height and shape of the text characters. Blank line insertion can be used in text mode only.

Each of these Vertical Compensation techniques can be controlled by programming the 82C455's Extension Registers. A combination of centering and stretching or blank line insertion may also be used.

SMARTMAP™

SMARTMAP™ is a proprietary feature that can be invoked to intelligently map colors to gray levels in text mode. SMARTMAP improves the legibility of flat panel displays by solving a common problem:

Most application programs are optimized for color CRT monitors using multiple colors. For example, a word processor might use a blue background with white characters for normal text, underlined text could be display in green, italicized text in yellow, and so on. This variety of colors, which is quite distinct on a color CRT monitor, can be illegible on a monochrome flat panel display if the colors are mapped to adjacent grayscale values. In the example, underlined and italicized text would be illegible if yellow is mapped to grayscale 4, green to grayscale 6 with the blue background mapped to grayscale 5.

SMARTMAP compares and adjusts the foreground and background grayscale values to produce adequate display contrast on flat panel displays. The minimum contrast value and the foreground/background grayscale adjustment values are programmed in the 82C455's Extension Registers. This feature can also be disabled completely.

VIDEO BIOS

In typical applications, the 82C455 is placed on the CPU board and the video BIOS is integrated with the system BIOS. A signal (ROMCS/) is provided for implementing a separate 8-bit ROM VIDEO BIOS. Chips and Technologies supplies a video BIOS that is optimized for the 82C455 hardware. The BIOS supports the extension functions of the 82C455, such as switching between the flat panel and the CRT, SMARTMAP™, Vertical Compensation, and palette load/save. The BIOS Modification Program (BMP) enables OEMs to tailor their feature set by programming the extension functions. Chips offers the BIOS as a standard production version, a customized version or as source code.

POWER-SAVING MODES

The 82C455 supports two power-down modes to reduce power consumption and extend battery-based operation. The first mode is the Relax mode, during which the display is blanked and the backlight (if used) can be turned off. While in the Relax mode, the 82C455 continues to generate video memory re-

fresh cycles and all display timing signals for the flat panel. The CPU has complete access to all the internal registers and to display memory. This mode is useful when the CPU is manipulating video data and updating display memory but no other user activity is occurring. Because the CRT Controller does not execute any DRAM cycles for the purpose of updating the display, power consumption in the DRAM is reduced. As an added benefit, the CPU can utilize the full display memory bandwidth while in this mode.

The second mode is the Retire mode, during which the 82C455 is invisible to the system. While in the Retire mode, the display is blanked, the display timing signals are halted and the flat panel should be turned off. The CPU cannot access any internal registers or display memory. During Retire, the 82C455 continues to refresh the DRAMs at a programmable rate, to conserve power in the display memory while preventing data loss. This mode is useful when system operation is suspended.

BUS INTERFACE

The 82C455 directly interfaces to 8-bit PC and PC/XT, 16-bit PC/AT and 8 or 16-bit MCA buses. All operations necessary to ensure proper operation in these various environments are handled in a fashion transparent to the CPU. These include internal decoding of all memory and I/O addresses, bus width translations, and generation of the necessary control signals.

The 82C455 interfaces directly to the CHIPS/250 and CHIPS/280, providing a simple, cost-effective solution for PS/2 compatible systems. When used with one of these CHIPSets, the 82C455 can execute FAST memory cycles at a speed greater than that normally available on the MCA bus.

DISPLAY MEMORY

The 82C455 supports a total of 256 Kbytes of display memory. The 82C455 serves as a DRAM controller for the system's display memory. It handles DRAM refresh, fetches data from display memory as required to refresh the screen, interfaces the CPU to display memory, and supplies all necessary DRAM control signals. The display memory is arranged as four planes of 64 Kbytes each. Each plane is eight bits wide for a total of 32 bits. Planes 0 and 1 share a common address bus, as do Planes 2 and 3. Each plane has a separate CAS signal and share a common RAS and write enable. Supported DRAMS include two 64Kx16 (with separate CAS or write enable signals), four 64Kx8 or eight 64Kx4. 120ns DRAMS are required for clock inputs up to 30MHz. Pseudo-Static and SRAMs can be supported with external address latches.

82C455 ARCHITECTURE

The 82C455 integrates four major internal modules:

Graphics Controller

The Graphics Controller interfaces the 8- or 16-bit CPU data bus to the 32-bit data bus used by the four planes (Maps) of display memory. It also latches and supplies display memory data to the Attribute Controller for use in refreshing the screen image. For text modes, this data is supplied in parallel form (character generator data and attribute code); for graphics modes, it is converted to serial form (one bit from each of four bytes form a single pixel). The Graphics Controller also performs any one of several types of logical operations on data while reading it from or writing it to display memory or the CPU data bus.

Sequencer

The Sequencer generates all CPU and display memory timing signals. It controls CPU access of display memory by inserting cycles dedicated to CPU access. It also contains mask registers which can prevent writes to individual display memory planes.

Attribute Controller

The Attribute Controller generates the 4-bit-wide video data stream used to refresh the display. This is created in text modes from a font pattern and an attribute code which pass through a parallel to serial conversion. In graphics modes, the display memory contains the 4-bit pixel data. In text and 16 color graphic modes the 4-bit pixel data acts as an index into a set of internal color look-up registers which generate a 6-bit stream. Two additional bits of color data are added to provide an 8-bit address to the external color palette. In 256 color modes, two 4-bit values are passed through the color look-up registers and assembled into an 8-bit value. Text and cursor blink, underline and horizontal scrolling are also the responsibility of the Attribute Controller.

CRT Controller

The CRT Controller generates all the sync and timing signals for the display and also generates the multiplexed row and column addresses used for both display refresh and CPU access of display memory.

MODES OF OPERATION

The 82C455 addresses the specific requirements of laptop design by providing different modes of operation to optimize power usage. The table at the bottom of the page summarizes these modes and display memory access in each.

Test Mode

This mode is entered when the RESET pin is low and the TEST pin is high. It is used for factory test purposes.

Reset mode

When this mode is activated by pulling the RESET pin high, the 82C455 is forced to VGA-compatible mode and the CRT is selected as the active display. In addition, the 82C455 is disabled; it must be enabled after deactivating the RESET pin by writing to the Global Enable Register (102h in Setup Mode). Access to all Extension Registers is also disabled. They must be explicitly enabled via the Extension Enable Register (103h in Setup Mode) following a reset. The RESET pin must be active for at least 64 clock cycles.

Setup Mode

In this mode, only the configuration registers are accessible (these include the Global Enable, Extension Enable and Global ID). In an MCA configuration, Setup mode is entered when the SETUP/ pin is low. This pin is typically controlled by bit-5 of port 94h and is implemented in system logic external to the 82C455. In a PC-bus implementation, Setup mode is entered by writing a 1 to bit-4 of port 46E8h. This port is incorporated in the 82C455. While in Setup mode, the video output is active if it was active prior to entering Setup mode and inactive if it was inactive prior to entering Setup mode.

Normal Operating Mode

In this mode all functions of the 82C455 are enabled except that the configuration registers are not accessible.

Relax and Retire Modes

The 82C455 supports two power-down modes to reduce power consumption and extend battery-based operation. The first mode is the Relax mode, during which the display is blanked and the backlight (if used) can be turned off. While in the Relax mode, the 82C455 continues to generate video memory refresh cycles and all display timing signals for the flat panel. The CPU has complete access to all the internal registers and to display memory. This mode is useful when the CPU is manipulating video data and updating display memory but no other user activity is occurring. Because the CRT Controller does not execute any DRAM cycles for the purpose of updating the display, power consumption in the DRAM is reduced. As an added benefit, the CPU can utilize the full display memory bandwidth while in this mode.

The second mode is the Retire mode, during which the 82C455 is invisible to the system. While in the Retire mode, the display is blanked, the display timing signals are halted and the flat panel should be turned off. The CPU cannot access any internal registers or display memory. During Retire, the 82C455 continues to refresh the DRAMs at a programmable rate to conserve power in the display memory while preventing data loss. This mode is useful when system operation is suspended.

Mode of Operation	RESET Pin	TEST Pin	PWRDN1 Pin	PWRDN2 Pin	Display Memory Access by CPU	Display Memory Access for Display Refresh
Test	Low	High	xxx	xxx	----	----
Reset	High	xxx	xxx	xxx	----	----
Setup	----	----	----	----	No	Yes
Normal	Low	Low	Low	Low	Yes	Yes
Relax	Low	Low	High	Low	Yes	No
Retire	Low	Low	Low	High	No	No

Note: Combinations of pin levels not shown in the table above are illegal and should not be used.

GENERAL PURPOSE OUTPUTS

The 82C455 provides two general purpose output pins. This feature relies on redefinition of the TRAP/ and ERMEN/ pins with the General Purpose Output Registers (XR08 and XR09). These pins can be defined to serve their normal function or can be individually 3-stated, forced low, or forced high. In most applications, the trap pin is used as a CRT / LCD control signal.

SCREEN BLANKING

The 82C455 permits blanking of the display by writing to bit-5 of the Sequencer Clocking Mode Register (SR01) or by pulling the PWRDN1 pin high. With the screen blanked, all memory cycles are available to the CPU except those used for display memory refresh. In addition, the video output can be forced to a pre-defined color (the default video) whenever the BLANK/ pin is asserted. This color is written to the Default Video Register (XR2B) (an Extension Register).

INTERNAL AND EXTERNAL PALETTES

The 82C455 contains 16 color look-up registers (in the Attribute Controller), each of which is 6 bits wide. These are used in 16 color modes to select 16 active colors from a palette of 64.

The 82C455 also supports an external palette DAC (Inmos IMSG176 or equivalent). CPU access to this device is controlled by the 82C455, which decodes CPU accesses and generates the PALRD/ and PALWR/ signals for the external palette. I/O addresses 3C6-3C9h are valid external palette addresses.

The internal color look-up table is always used in CRT modes and can be optionally used in the flat panel modes. The external palette is used only with analog CRTs. It is not used with digital CRTs and flat panels.

LIGHT PEN REGISTERS

In the CGA and Hercules modes, the contents of the Display Address counter are saved at the end of the frame before being reset. The saved value can be read in the CRT Controller Register space at indices 10h and 11h. This allows simulation of a light pen hit in CGA and Hercules modes.

SYSTEM TRAPS

The 82C455 supports generation of traps (NMIs) on one or more conditions. The Trap Enable and Trap Status Registers (XR16 and XR17) are utilized to implement this feature. Note: the use of traps with OS/2™ and other operating environments may cause problems.

FRAME INTERRUPTS

The 82C455 supports frame interrupts in a manner compatible to either the PC bus or MCA bus. For compatibility with the IBM VGA adapter in the PC bus, frame interrupts may also be disabled through the Emulation Mode register (XR14).

DIP SWITCH INPUTS

The 82C455 supports up to 7 DIP switch inputs. These can be read through the Dip Switch Register (XR01). To implement this feature, the A16, A17, A18, BHE/, ADDHI, AEN (MIO/) and RFSH/ (VGAENAB) pins are connected to the 7 DIP switches through a multiplexer. These inputs can be used to define initialization conditions. Note: the standard CHIPS BIOS does not require that any DIP switches be connected to these inputs.

CONTEXT SWITCHING

For support of multi-tasking, windowing and context switching operating environments, the entire state of the 82C455 (internal registers) is read- and write-able. This feature is 100% compatible with IBM's VGA.

WRITE PROTECTION

A Feature of the 82C455 is the ability to write protect most of the standard VGA registers. This feature is used to provide backwards compatibility with software written for older generation display types. The write protection is grouped into register sets and controlled by the Write Protect Register (XR15).

82C455 Pinouts